

1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%. 2. ALL CAPACITANCE VALUES ARE IN MICROFARADS. 3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.	REV	ECN	DESCRIPTION OF REVISION	CK APPD DATE
	6	0031723518	ENGINEERING RELEASED	2021-10-03

X2203/MLB

LAST_MODIFICATION=Sun Oct 3 21:59:49 2021

LAST_MODIFICATION=Sun Oct 3 21:59:49 2021

LAST_MODIFICATION=Sun Oct 3 21:59:49 2021

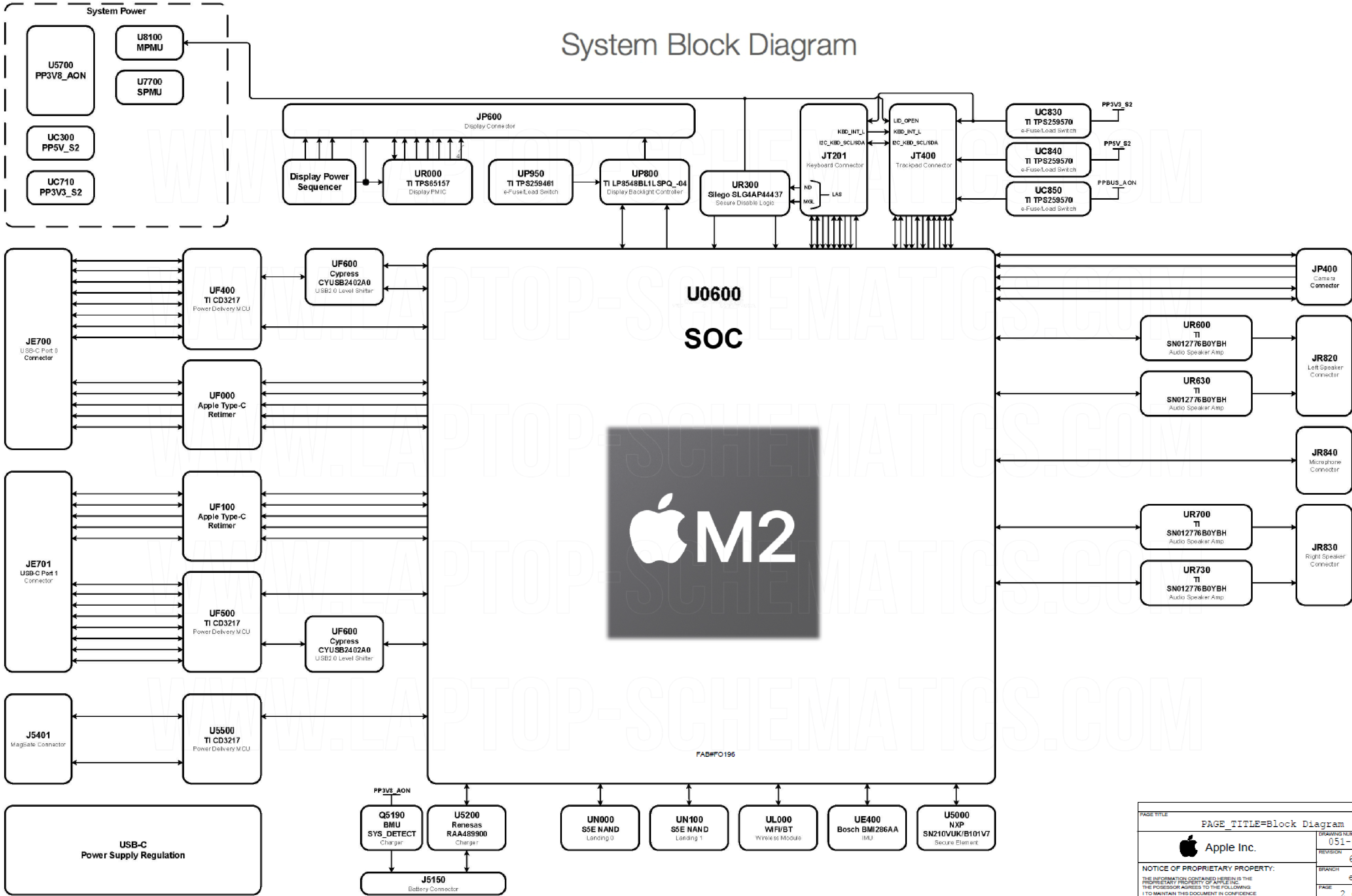
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System Block Diagram



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A BOM Groups

BOM GROUP	BOM OPTIONS
MLB_COMMON	SCHEM,PCBF,COMMON,MLB_PROGPARTS,MLB_USBC,MLB_POWER,MLB_PMU,MLB_MECH,MLB_MISC,MLB_BLC,MLB_TCON,MLB_WIRELESS,EVT
MLB_USBC	ATCRTMR:B0,USBCPC:LAPTOP_B3,RT13_EFUSE:VDDIO,EUSB_LS:B0,ACE_WILL_BE_OTPED:YES,LPKA_TEST_MODE:YES
MLB_PROGPARTS	SOC_ROM:BLANK,RT13_ROM:BLANK,SE:DEV_SW_LN,UPC01_ROM:EVT,UPC5_ROM:EVT
MLB_POWER	P3V8AON_IC:A2_R170,P3V8AON_LPM,WHAMOLA:0A5~13V7,P5VS2PWREN_BYPASS:NO
MLB_PMU	MPMU_IC:A0_JPI,SPMU_IC:A0_JPI,PMU_BULK_VDDQL,PMU_32K_CLK:XOSC,PMU_FB:FF,BUCK6_BULK_REG
MLB_MECH	SHLD_CAN_MLB:EVT,BRKT_KBD:EVT
MLB_MISC	BOARD_ID,TPAD_32KCLK:NO,SYSDCT:PKT,BOOT_CPU_0,PMU_OUT32K:WLBT,SENSOR_IMU,MIPI_PMR:NO,REFIMU_IC:RM1284,Q5369_DLY:YES,SOC_RU706:Q0BM,OCELOT_BYPASS:100NF
MLB_DEV	SENSORS:DEV,DEVELOPMENT,USBC_DBG,BTN_DBG
MLB_BLC	BLC_BEN_IC:V8,BLC_5V_CAP:4P7_UF,BLC_5V_SERIES:10_OHM,BLC_KBD_BOOST_USED:NO
MLB_TCON	PMIC_SDG_VBUCK1:NO,SDG_TI_PROG:X2203,SDG_TI
MLB_WIRELESS	RF-CONN

B Build Specific Groups

BOM GROUP	BOM OPTIONS
BOARD_ID	BOARD_ID_3
PROTO0	BOARD_REV_3,BOARD_REV_2,BOARD_REV_1,BOARD_REV_0
PROTO1	BOARD_REV_3,BOARD_REV_2,BOARD_REV_1
PROTO1B	BOARD_REV_3,BOARD_REV_2,BOARD_REV_0
PROTO2	BOARD_REV_3,BOARD_REV_2
PROTO2B	BOARD_REV_3,BOARD_REV_1,BOARD_REV_0
EVT	BOARD_REV_3,BOARD_REV_1
DVT	BOARD_REV_3,BOARD_REV_0
PVT	BOARD_REV_3

Pull-ups: BOARD_ID[7:0] = 8'b0010_1000

Pull-downs: 4'b0000

Pull-downs: 4'b0001

Pull-downs: 4'b0010

Pull-downs: 4'b0011

Pull-downs: 4'b0100

Pull-downs: 4'b0101

Pull-downs: 4'b0110

Pull-downs: 4'b0111

C DC/DC BOM Groups

BOM GROUP	BOM OPTIONS
DCDC_COMMON	SCHEM,PCBF,COMMON,MLB_POWER,MLB_PMU,MLB_MECH,MLB_MISC,MLB_BLC,EVT

D RF BOM Groups

BOM GROUP	BOM OPTIONS
RF_COMMON	SCHEM,PCBF,RF-CONN

E Top-Level APNs

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
051-07020	1	SCHEM,MLB,X2203	SCHEM	CRITICAL	SCHEM
820-02536	1	PCBF,MLB,X2203	PCBF	CRITICAL	PCBF
685-00426	1	COMMON PARTS,MLB,X2203	CBOM	CRITICAL	CMN_PARTS_BOM
685-00427	1	NAND1,MLB,X2203	P1BOM	CRITICAL	PARTS_SSDNAND1
985-01536	1	DEV PARTS,MLB,X2203	DEV1	CRITICAL	DEV_PARTS_BOM

F Reference Design Pack Options

USB-C

PACK_OPTIONS TO INCLUDE IN NETLIST
USBC_SPI_UPC0
USBC_DEBUG_UPC0
USBC01_VR5V_LOCAL_NO
USBC_LAPTOP
PKGS:SMALL_PITCH
USBC_LAPTOP_CC_PRT
ACE2_SS_CAP
USBC_SPI_NO_2ND_ROM
USBC_SPI_UPC0_AND_NO_2ND_ROM
ACTIVE_READY:SMALL_PITCH_CHECK_WITH_DPM
INV:DPW

Iceman VR

PACK_OPTIONS TO INCLUDE IN NETLIST
3V8_AON_PBUS-18V
3V8_AON_I2C-DEV
3V8_INDUCTOR:1P5MM
3V8_AON_MLCC-LN

Wireless

PACK_OPTIONS TO INCLUDE IN NETLIST
SUNWAY
WLBT_D2R_TP_STATEN
WLBT_TP_0P2

Audio

PACK_OPTIONS TO INCLUDE IN NETLIST
SPKRAMP_A
SPKRAMP_B
SPKRAMP_D
SPKRAMP_E
SPKRAMP_ICC_GB

PP3V3_S2 VR

PACK_OPTIONS TO INCLUDE IN NETLIST
3V3_S2_PBUS-18V
3V3_S2_MLCC-LN
3V3_S2_VOUT-B12

Charger

PACK_OPTIONS TO INCLUDE IN NETLIST
CHGR_72W
CHGR_PBUS18V
CHGR_MLCC-LN

PP5V_S2 VR

PACK_OPTIONS TO INCLUDE IN NETLIST
5V_S2_PBUS18V
5V_S2_VOUT-B12
5V_S2_IND-15
5V_S2_MLCC-LN
5V_S2_THINSTNCL

Display Backlight

PACK_OPTIONS TO INCLUDE IN NETLIST
BLC_CBULK:0603
BLC_FET:OFF
BLC_IND:10UH
PANLEWR_MINNIE
BLC_FERRITE:YES

SOC

PACK_OPTIONS TO INCLUDE IN NETLIST
SOC_MIPI_ENABLE
SOC_MIPI_1SIDE
ONE_SIDED
PCI_E_GPO
LPDP_INT_RCAL
LPDPFX0_RCAL
OCELOT_BYPASS:100F

NAND

PACK_OPTIONS TO INCLUDE IN NETLIST
SSD_4_3UF_0402THIN


PMU

PACK_OPTIONS TO INCLUDE IN NETLIST
TPAD32K:PMU
PMU_32K_MEMS
PMU_32K_XOSC

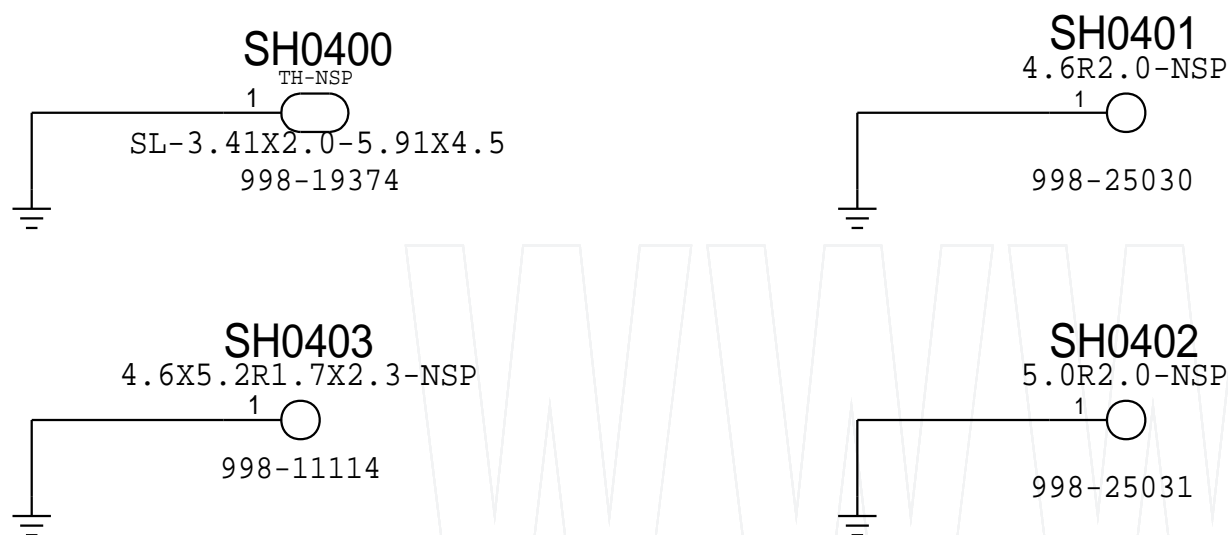
IMU

PACK_OPTIONS TO INCLUDE IN NETLIST
REFIMU_VDD:LCFILT
REFIMU_TEST:NO

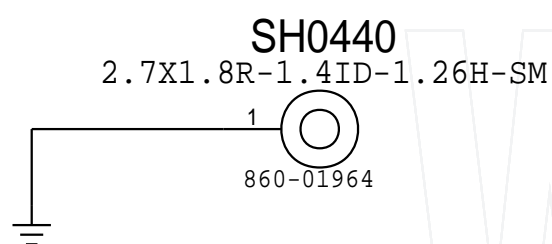
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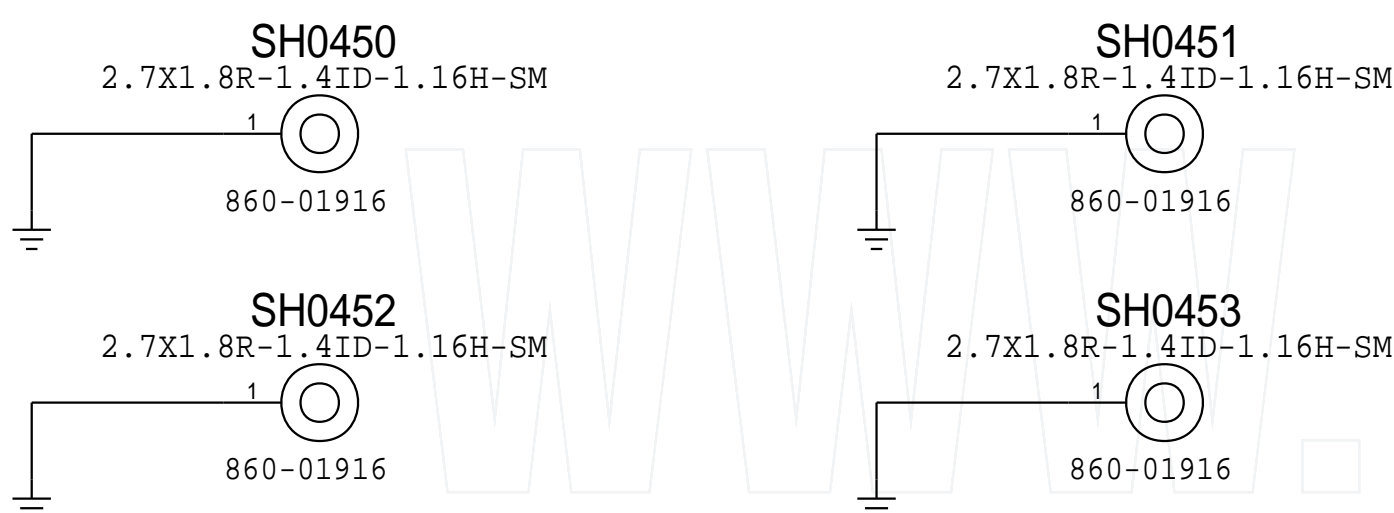
A Mounting Holes



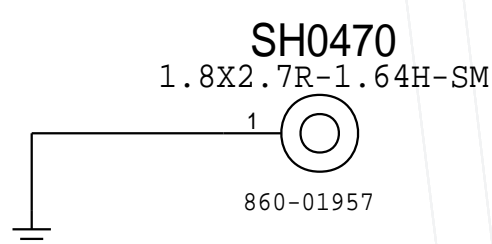
B MDB Cowling Bosses



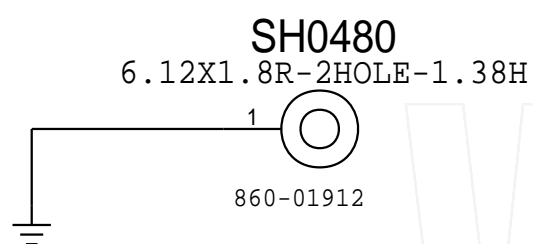
C MagSafe/USB-C Cowling Bosses



D WiFi Module Cowling Boss

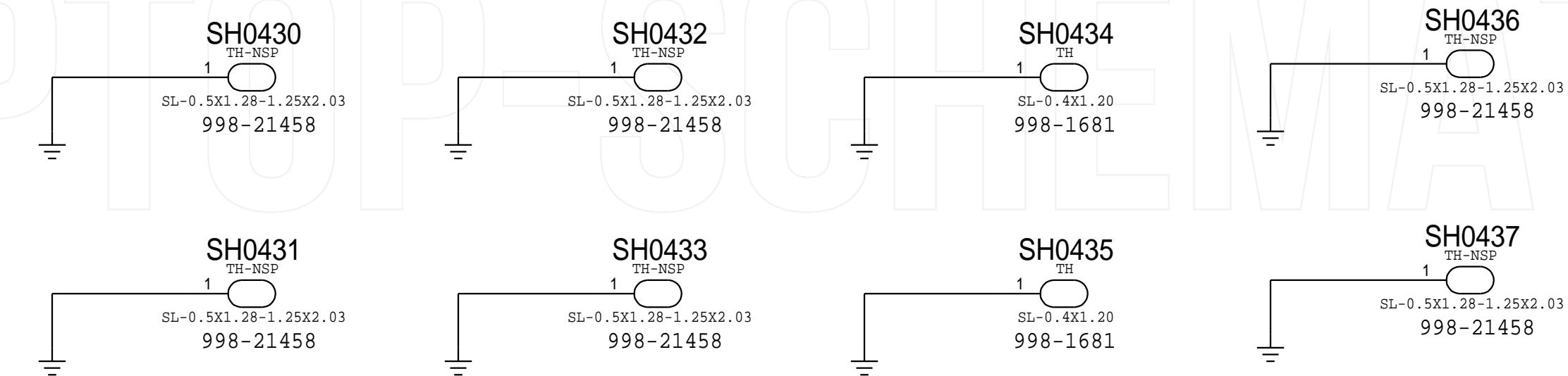


E Right Speaker Cowling Boss

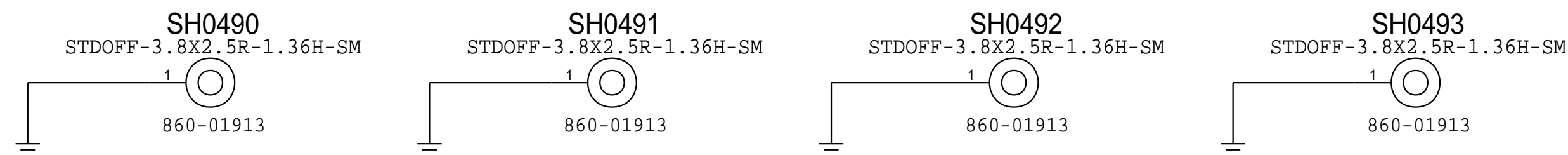


F MLB Shield Fence

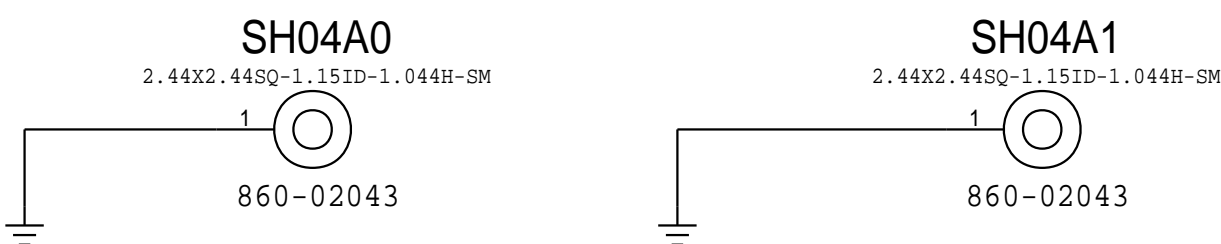
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
806-32496	1	SHIELD,FENCE,THERMAL,MLB,P1,X2147	SHLD1	CRITICAL	SHLD_CAN_MLB:P2
806-35214	1	FENCE,MLB,EVT,X2147	SHLD1	CRITICAL	SHLD_CAN_MLB:EVT



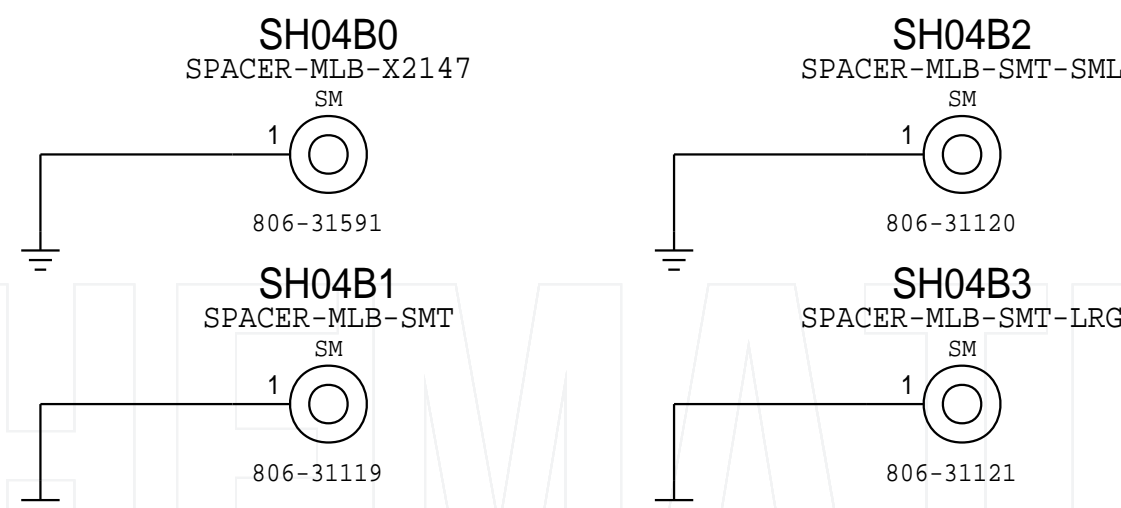
G SOC Thermal Module Bosses



H Antenna Cowling Bosses



I Spacers



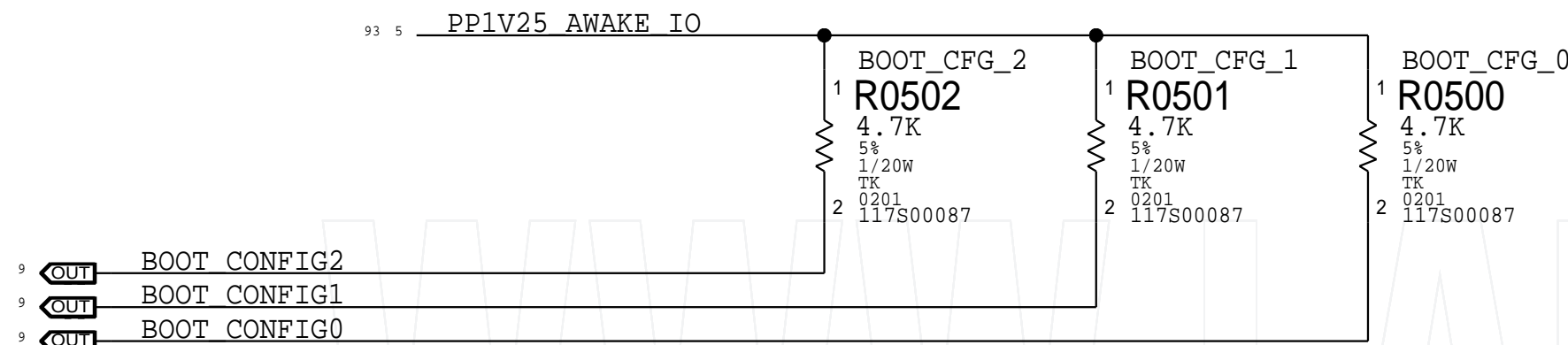
J Keyboard Bracket

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
806-32523	1	BRKT,MLB,SMT,X2147	BRKT1	CRITICAL	BRKT_KBD:P2
806-35209	1	BRKT,MLB,EVT,X2147	BRKT1	CRITICAL	BRKT_KBD:EVT

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BOM_COST_GROUP=MECHANICALS

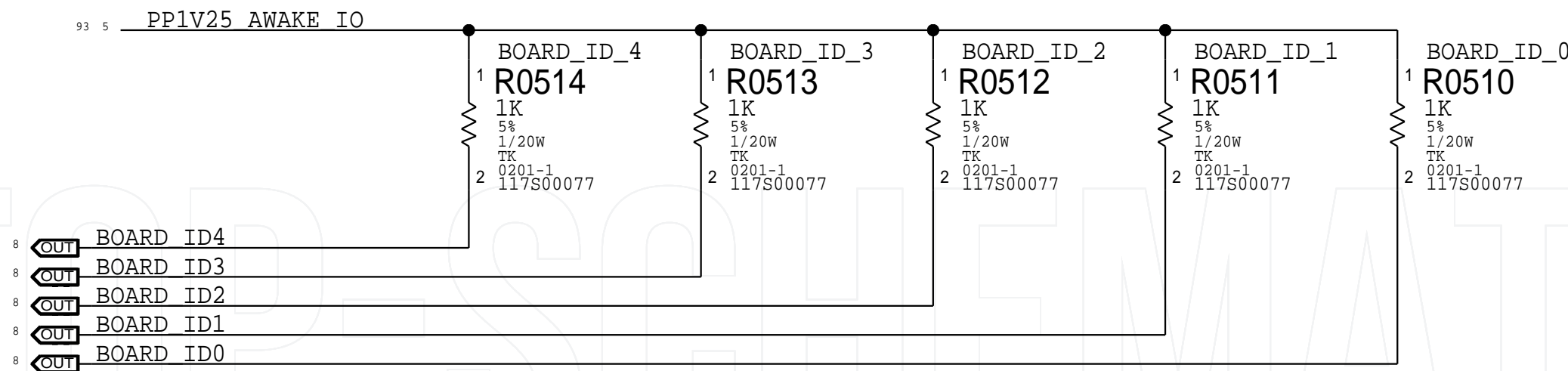
A BOOT CONFIG ID



STATEN BOOT AND POWER uARCH SPEC 2.1.5 (Section 2.2, Table 2.3):

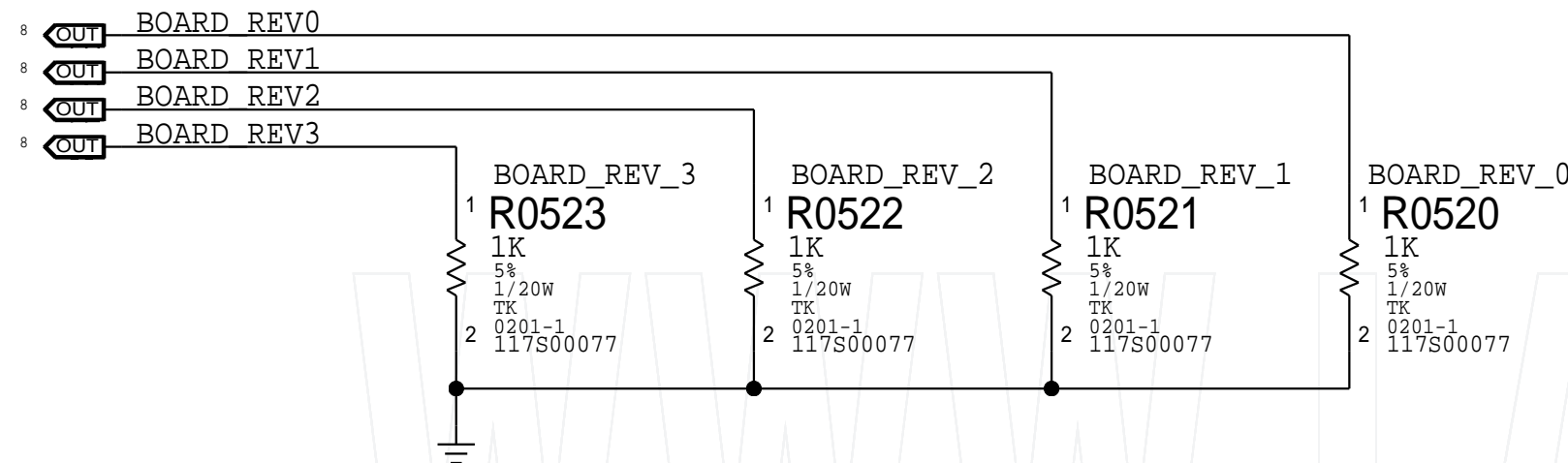
BOOT_CFG[2:0]	MODE
000	NAND, 1.2V SPI0, 12MHZ, TESTMODE
001	NOR, 1.2V SPI1, 40MHZ
010	NAND, 1.2V SPI0, 12MHZ
011	NAND, 1.2V SPI0, 40MHZ
100	NOR, 1.2V SPI1, 12MHZ, TESTMODE
101	NOR, 1.2V SPI1, 40MHZ, TESTMODE
110	NOR, 1.2V SPI1, 6MHZ, TESTMODE
111	NOR, 1.2V SPI1, 12MHZ

B BOARD ID




- BOARD_ID[7:0] assignments by product at link in QR Code.
- BOARD_ID[7:5] come from SOC
- BOARD_ID[4:0] are straps on MLB, sampled 100US after cold reset deassert.
- Staten Boot Power Micro Architecture Spec 2.1.3

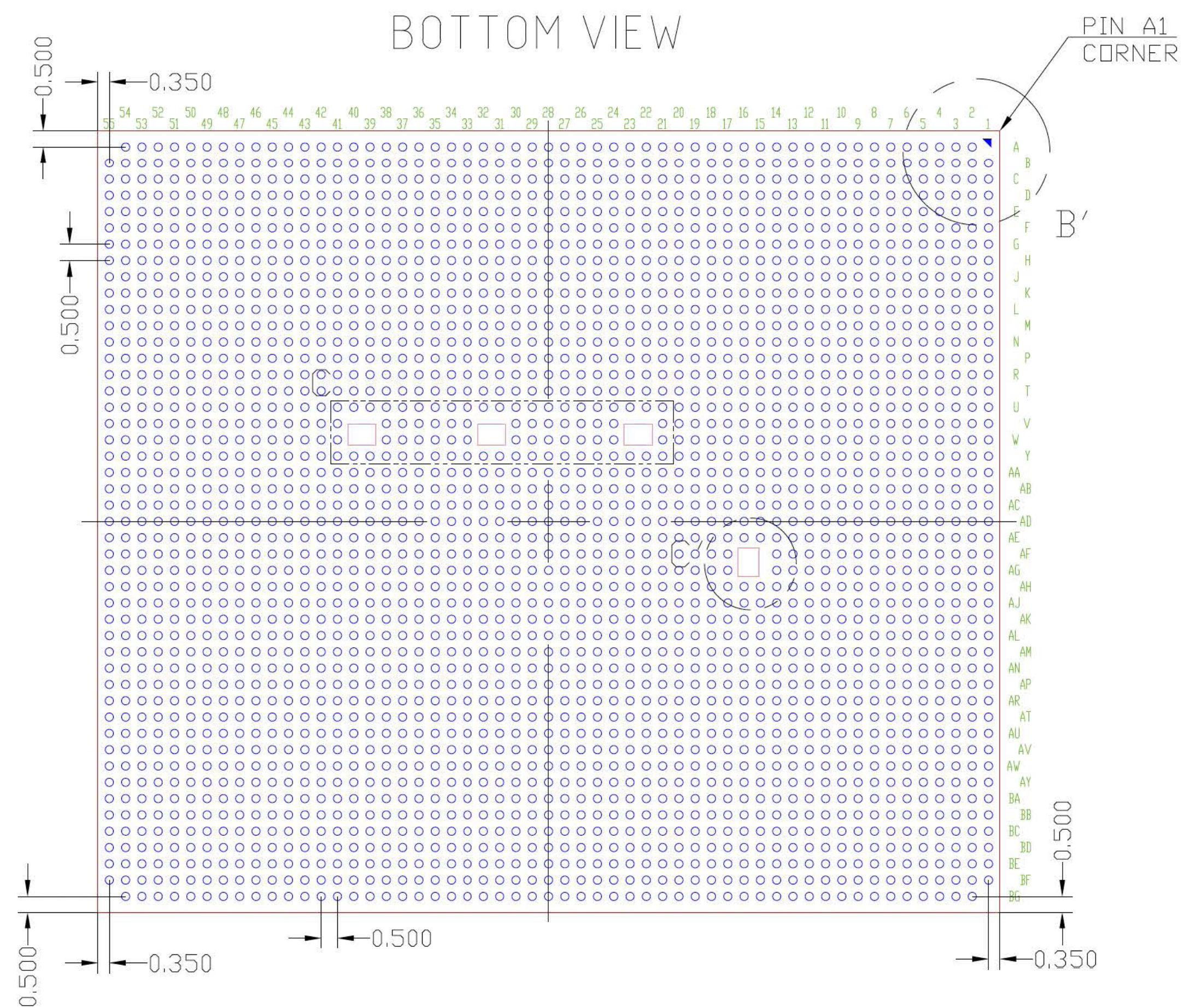
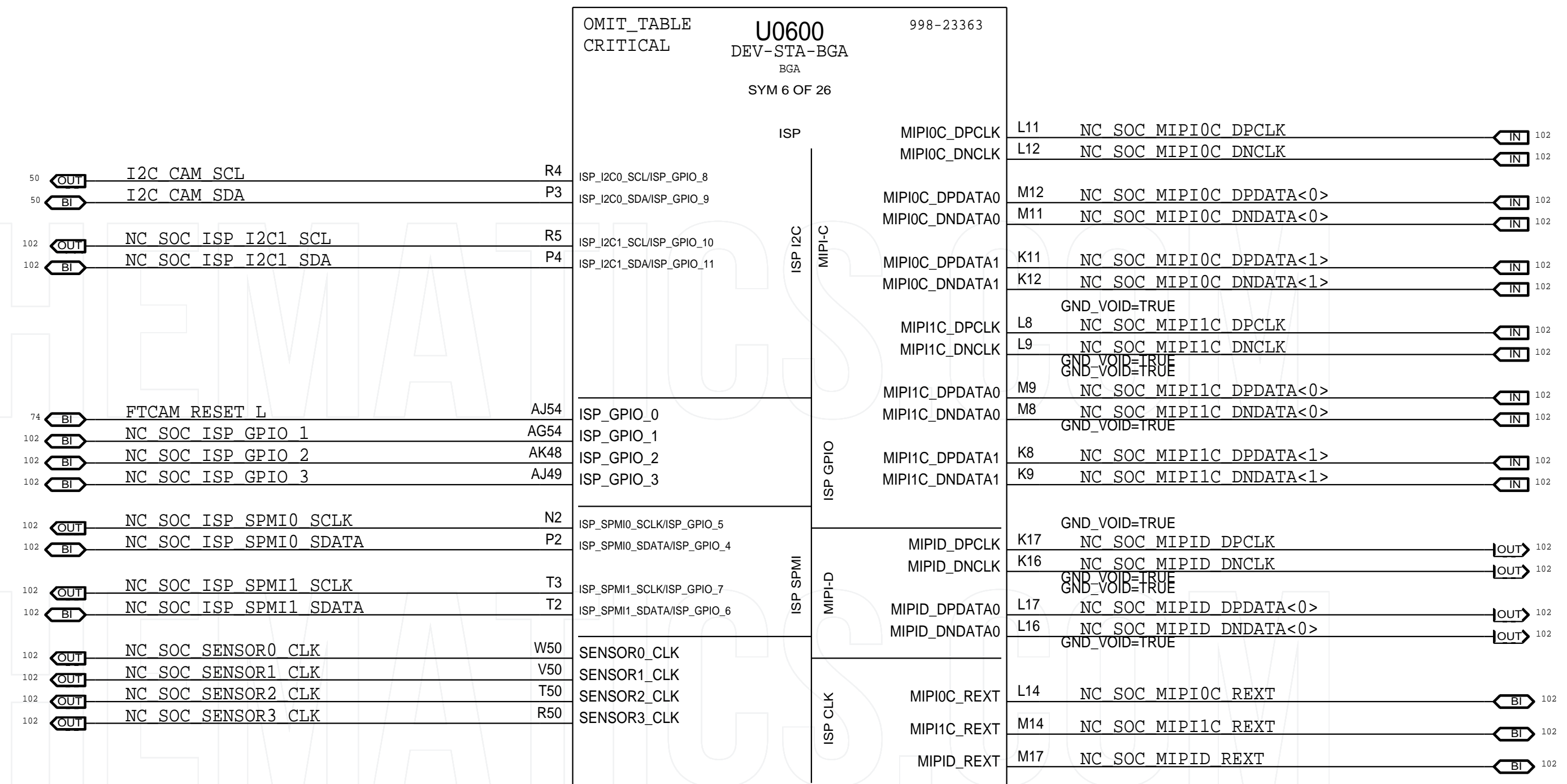
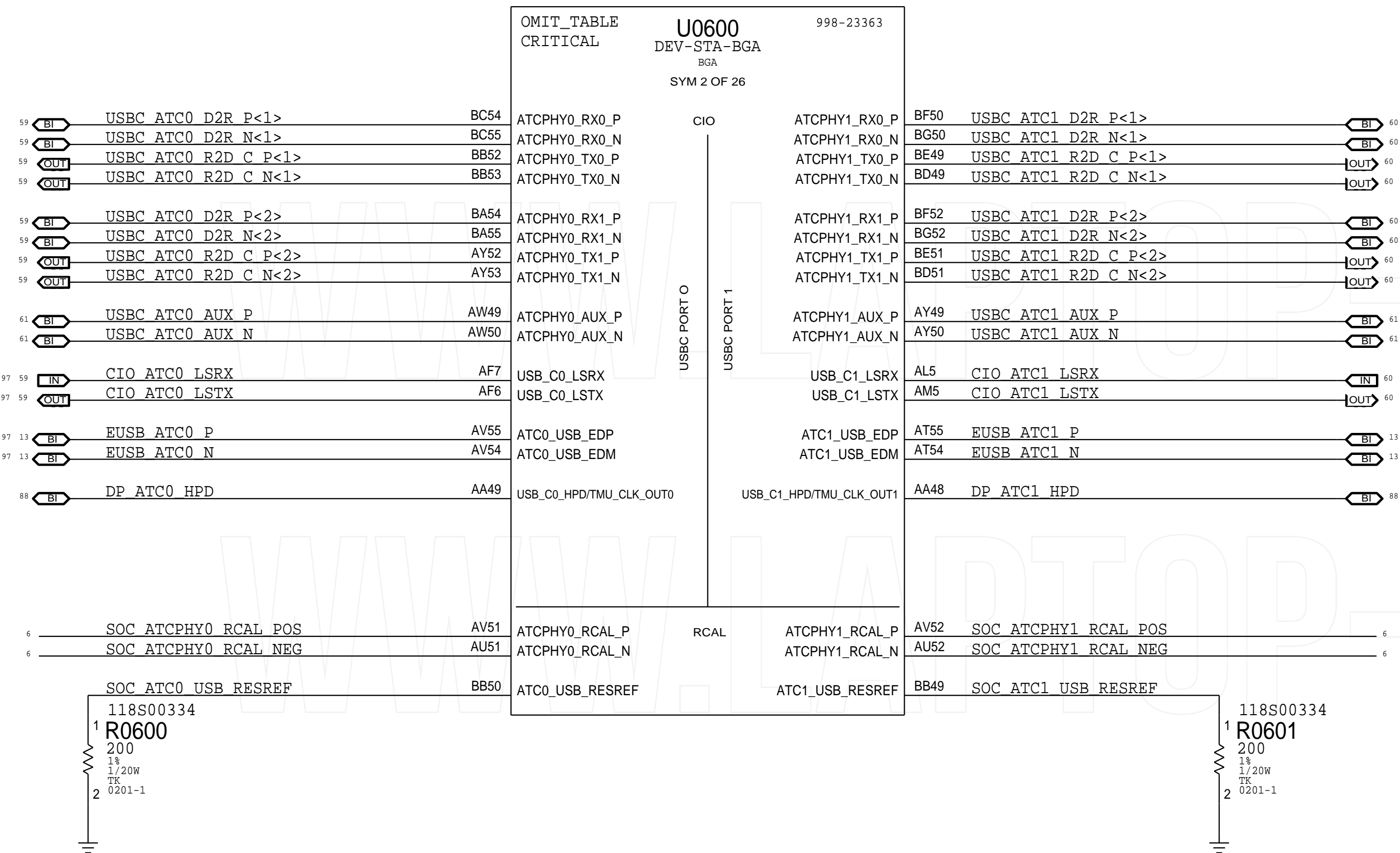
C BOARD REV



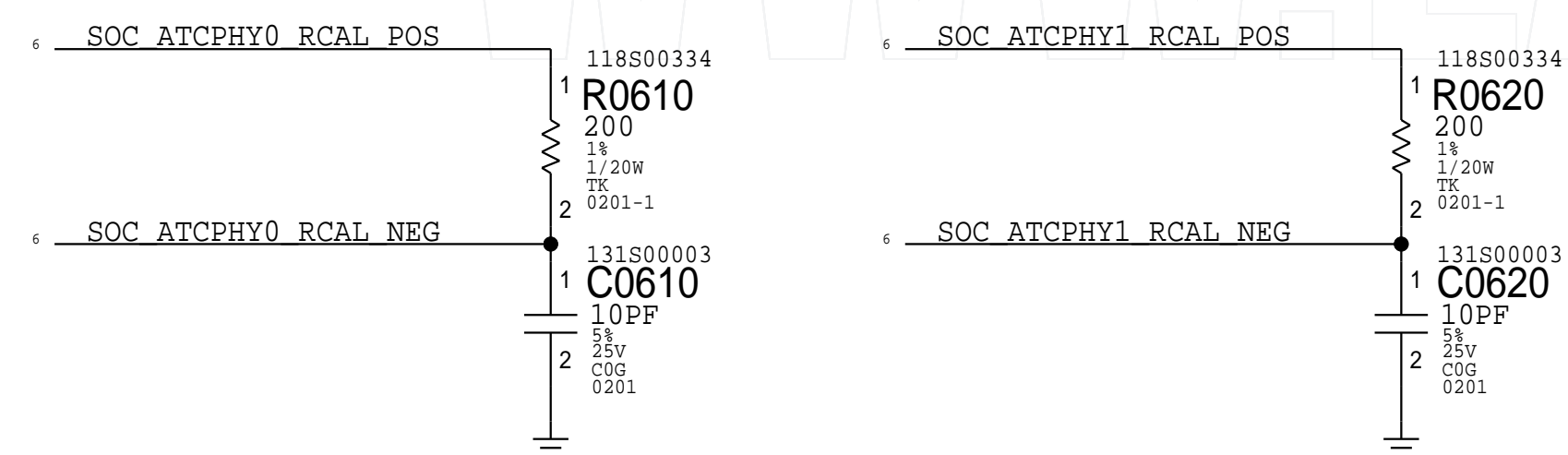
- Stuffing the Resistor Results in a Logic Low (1'b0)


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SOC: CONFIG STRAPS						
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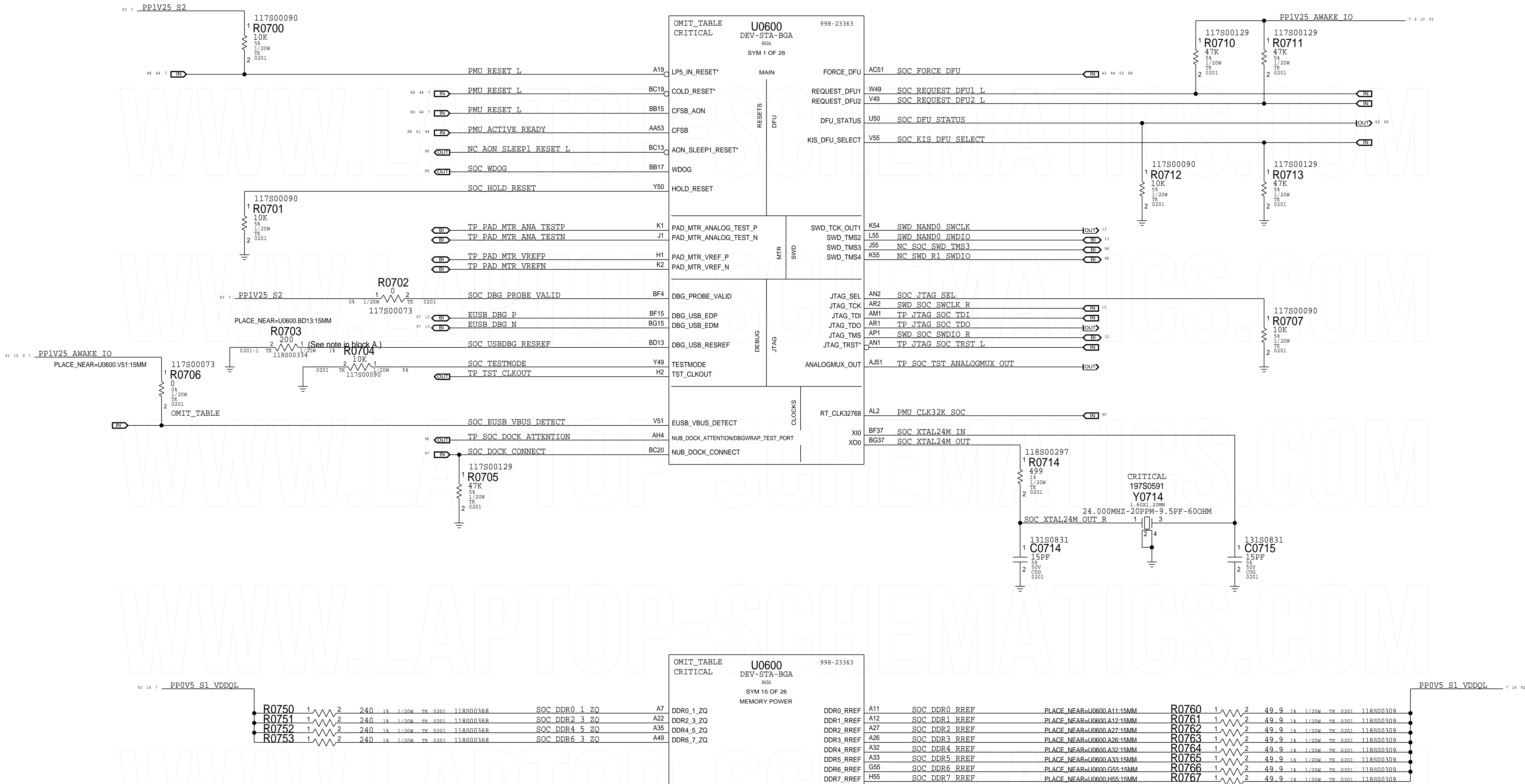
BOM_COST_GROUP=SOC



Ⓐ Termination Resistance Calibration (RCAL)



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A RESREF Notes

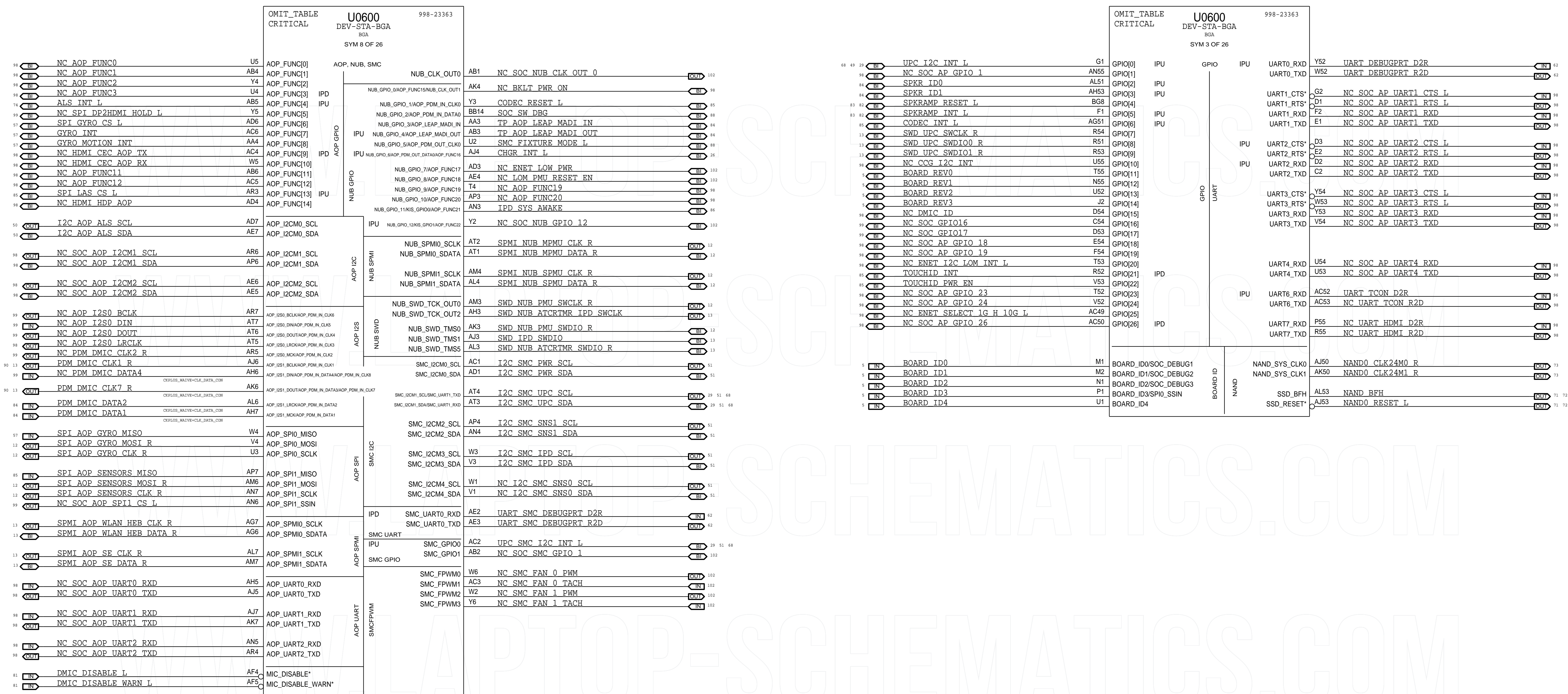
- The RESREF node is sensitive to noise.
- 1-sided PCBs may be able to place R0703 less than 15mm from SOC pin on the perimeter of the SOC.
- 2-sided PCBs may be able to place R0703 less than 5mm from SOC pin.

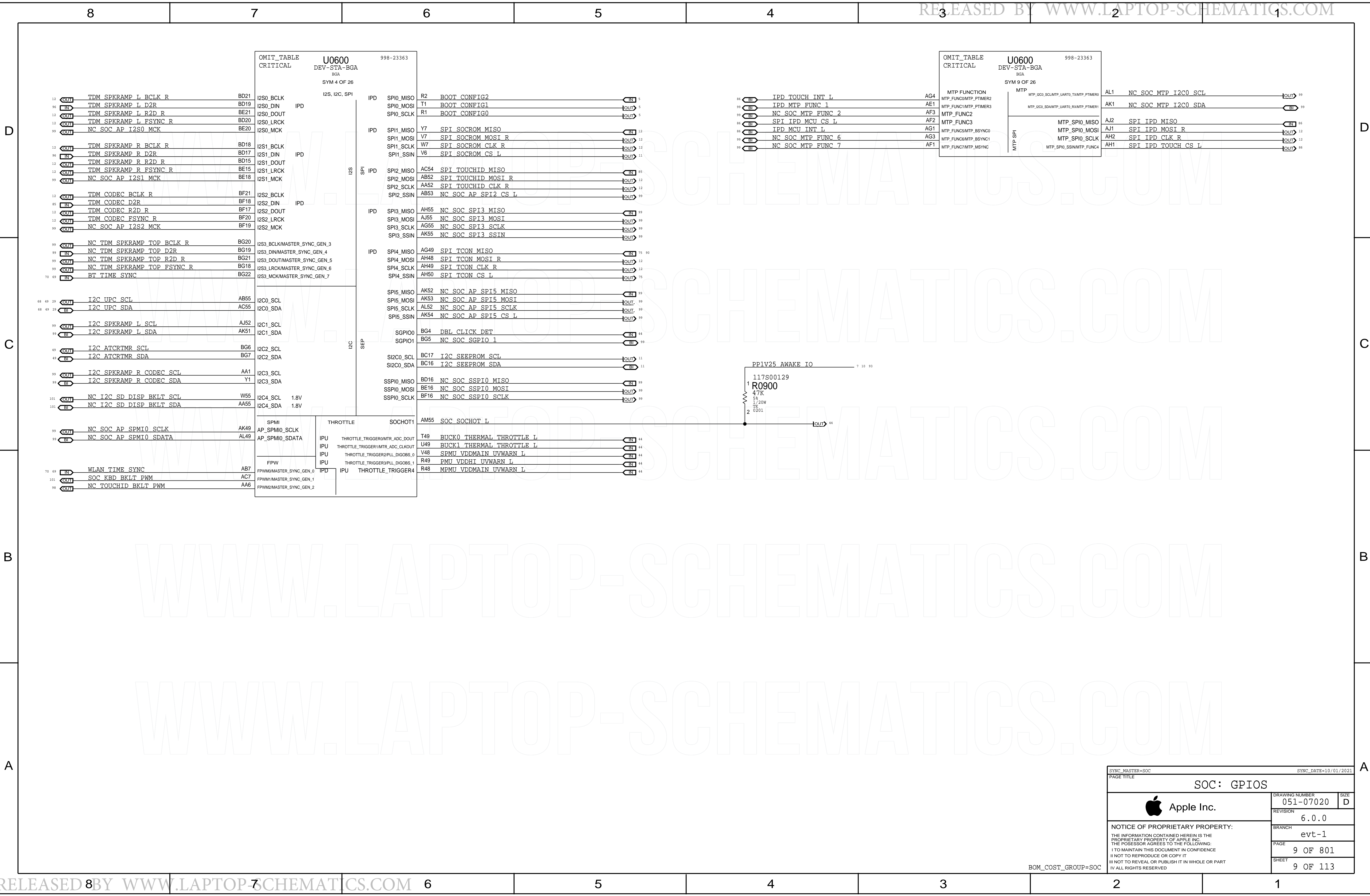
B EUSB_VBUS_DETECT BOM Table

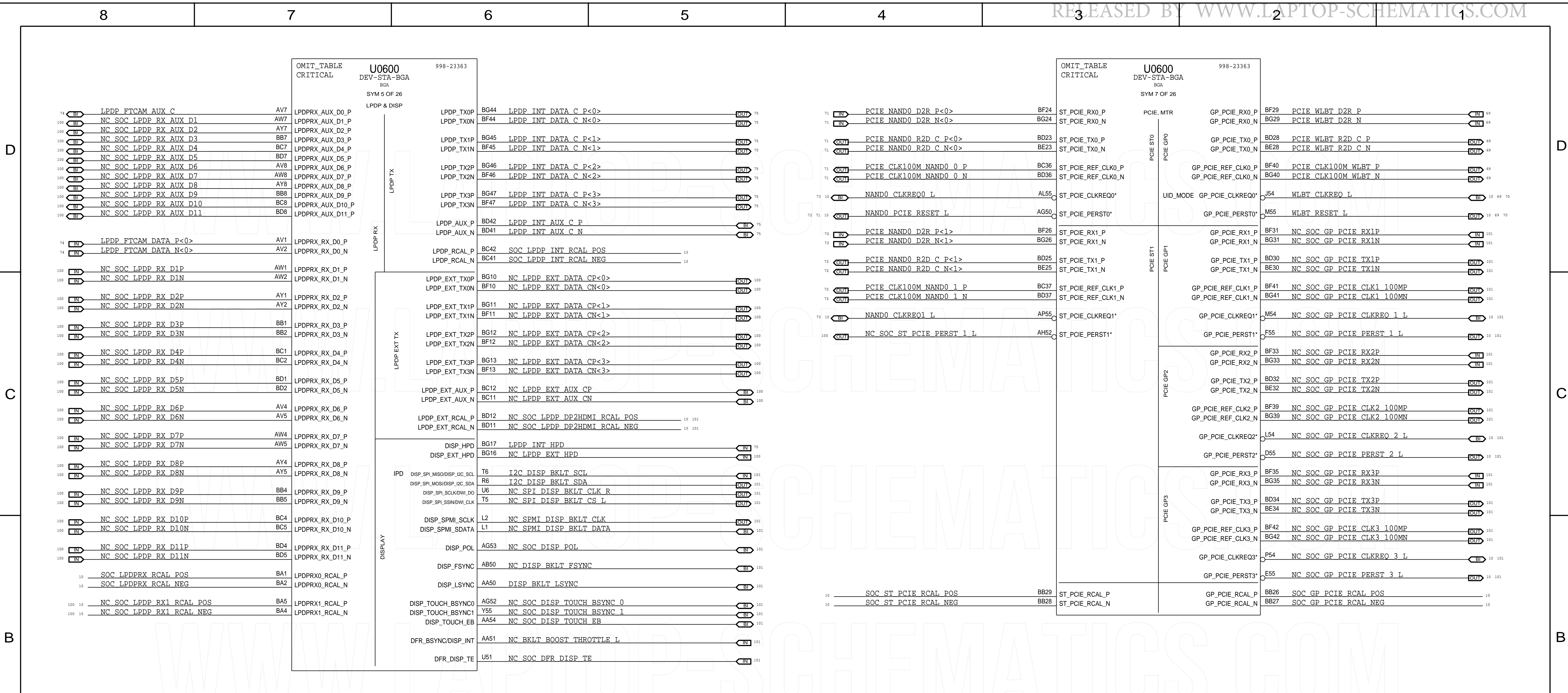
PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
117S00090	1	RES,TX,10K OHM,5%,1/20W,0201	R0706	SOC_R0706:10KOHM
117S00073	1	RES,TX,0 OHM,1A MAX,1/20W,0201	R0706	SOC_R0706:0OHM

SYNC_MASTER=SOC			SYNC_DATE=10/01/2021		
PAGE TITLE			SOC: RESETS, DEBUG, MISC		
			DRAWING NUMBER	051-07020	SIZE
			REVISION	6.0.0	D
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			PAGE	7 OF 801	
			SHEET	7 OF 113	

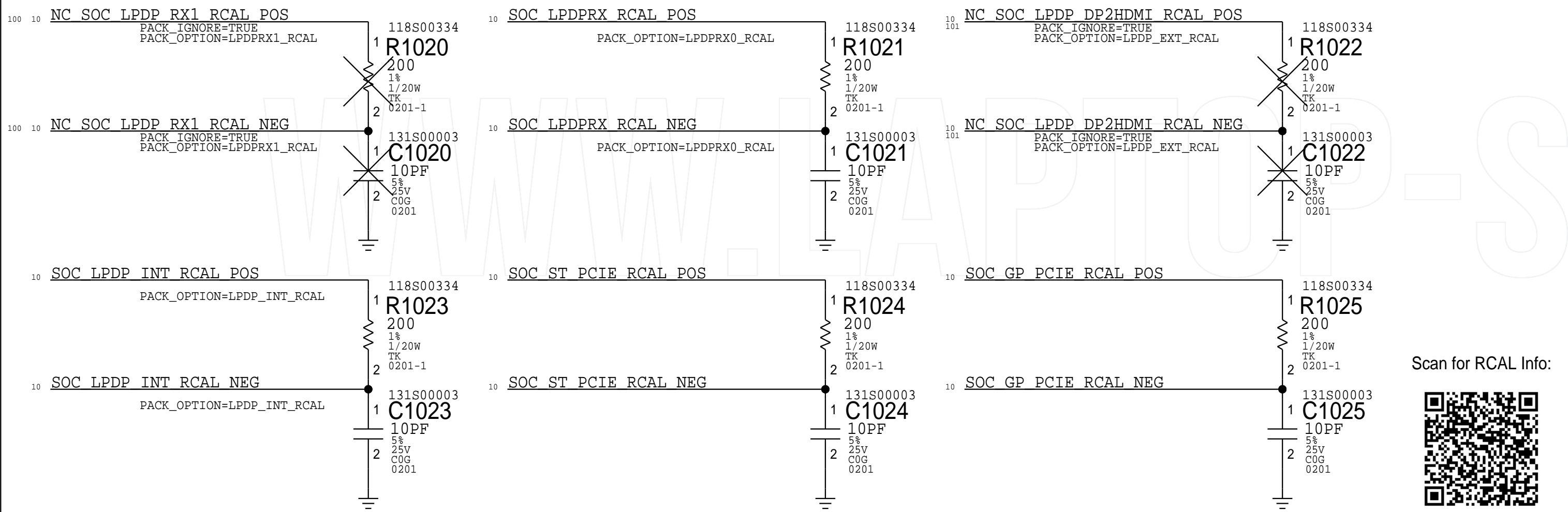
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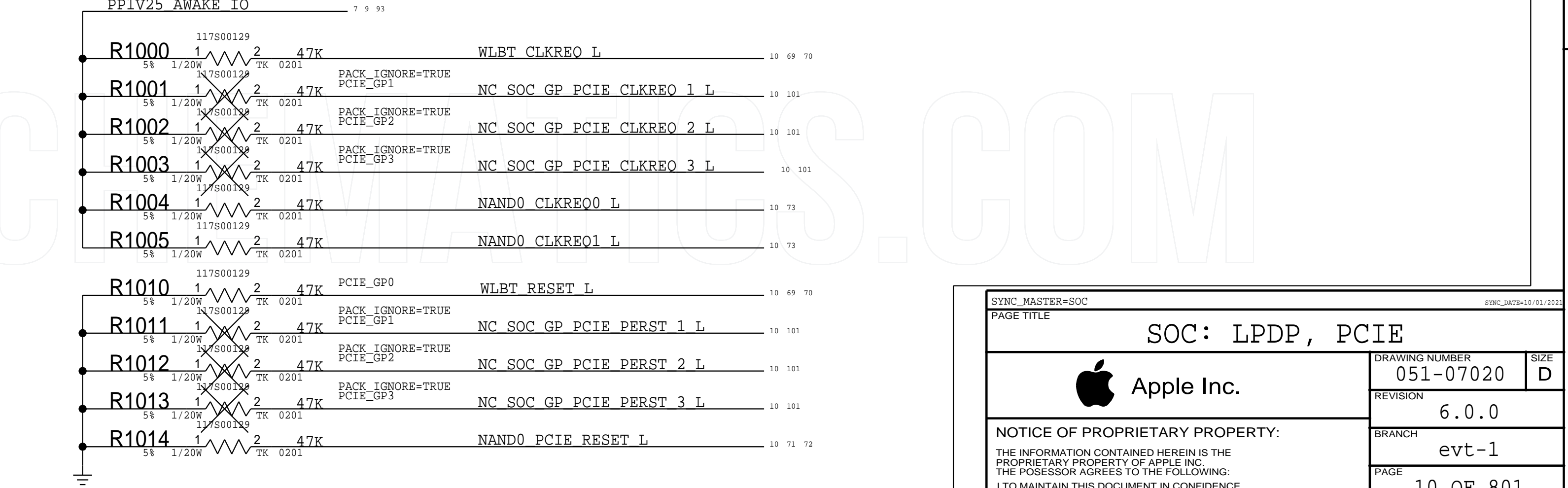




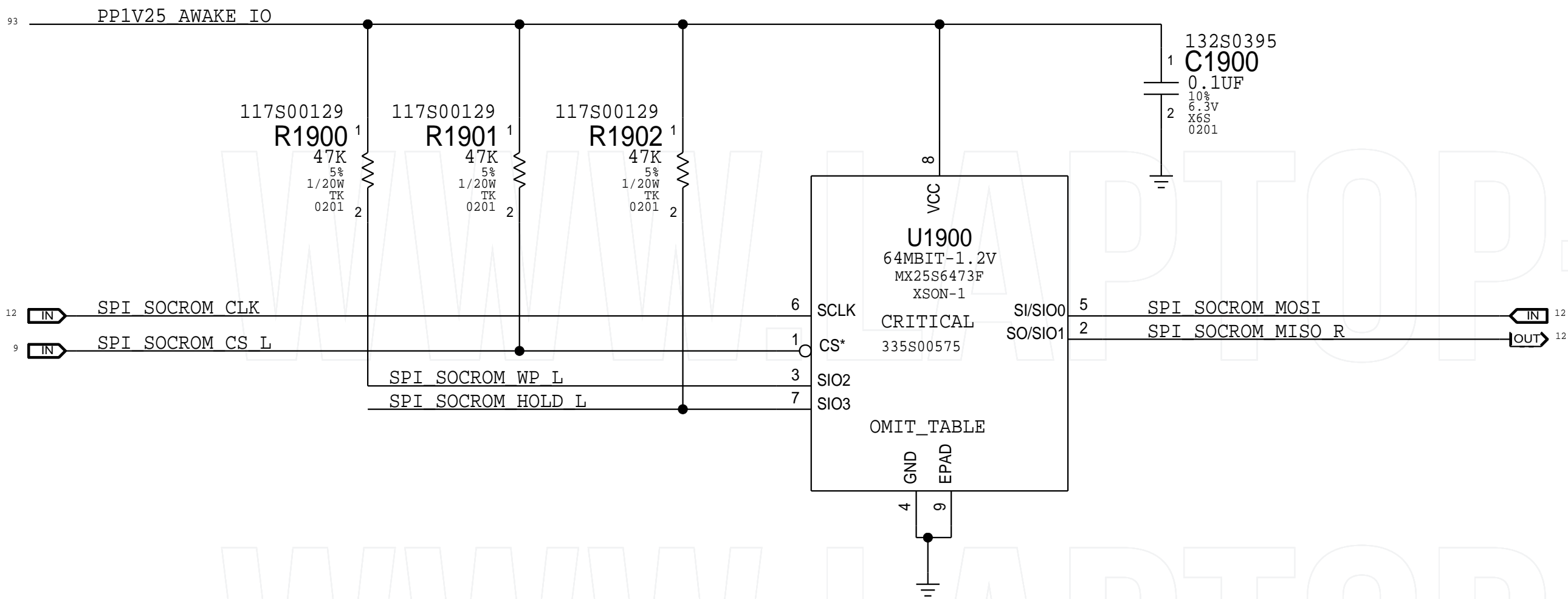
A Termination Resistance Calibration (RCAL)



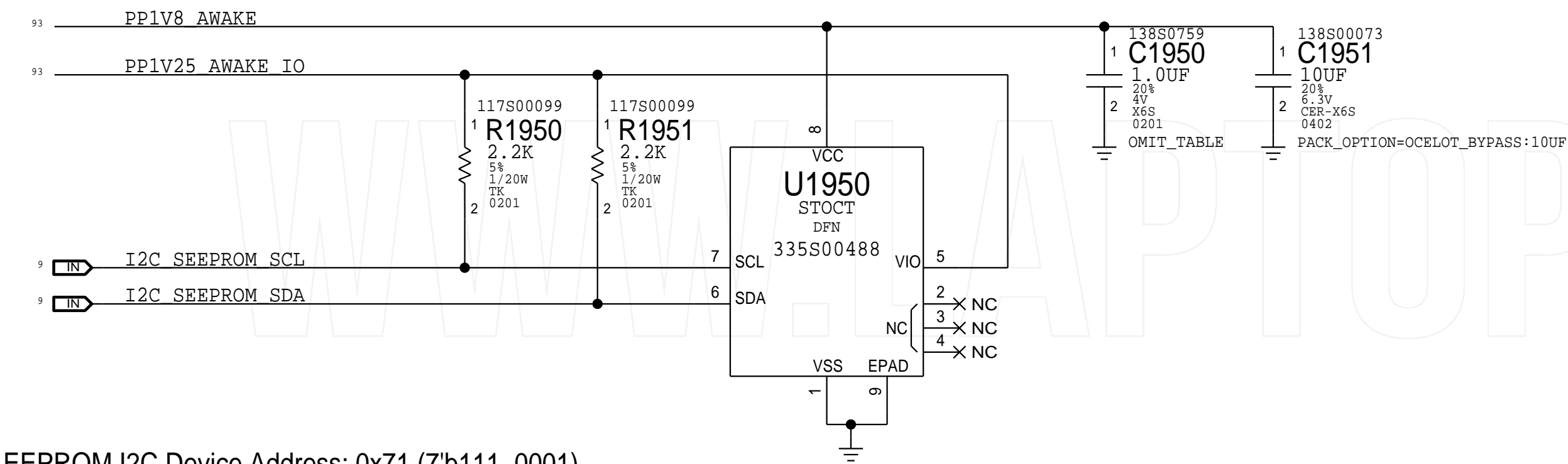
B PCIe CLKREQ/PERST Pull-Ups/Downs



A SPI ROM



B SEP EEPROM



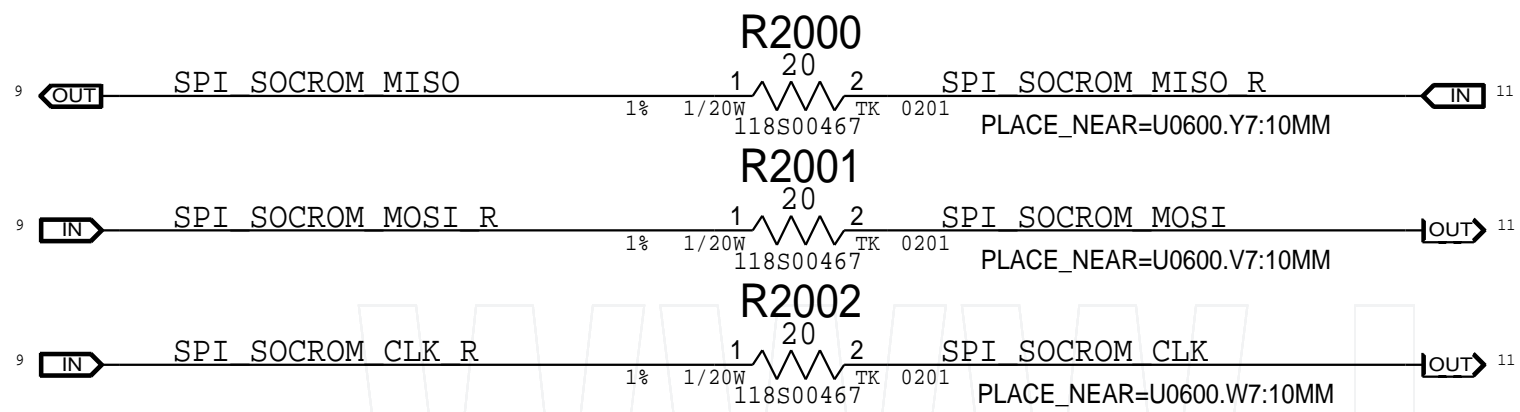
SEP EEPROM I2C Device Address: 0x71 (7'b111_0001)

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
138S0759	1	CAP,CER,1UF,20%,4V,X6S,0201	C1950		OCELOT_BYPASS:1UF
132S0395	1	CAP,CER,0.1UF,10%,6.3V,X6S,0201	C1950		OCELOT_BYPASS:100NF

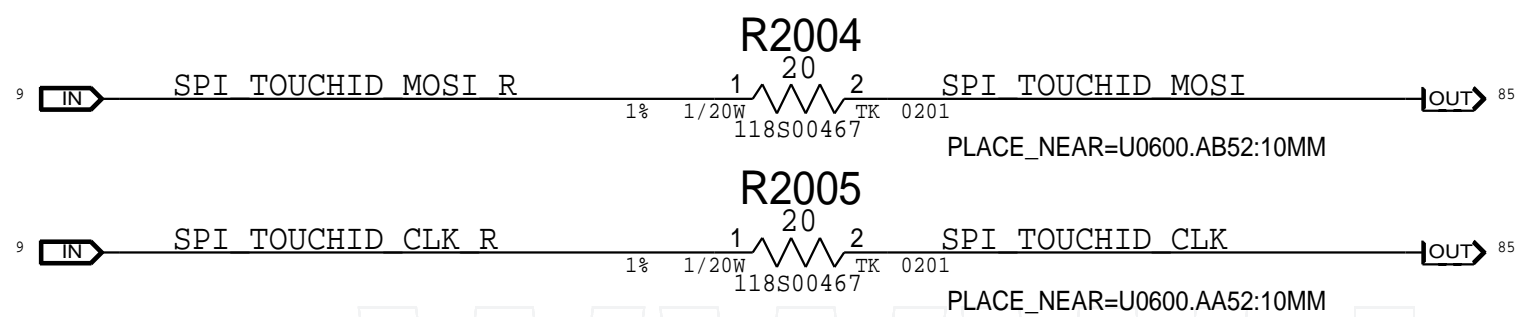
PAGE TITLE			DRAWING NUMBER			SIZE		
SOC: SPI NOR, SEP ROM			051-07020			D		
Apple Inc.			REVISION			6.0.0		
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I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE			SHEET			11 OF 113		
II NOT TO REPRODUCE OR COPY IT								
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART								
IV ALL RIGHTS RESERVED								

BOM_COST_GROUP=SOC

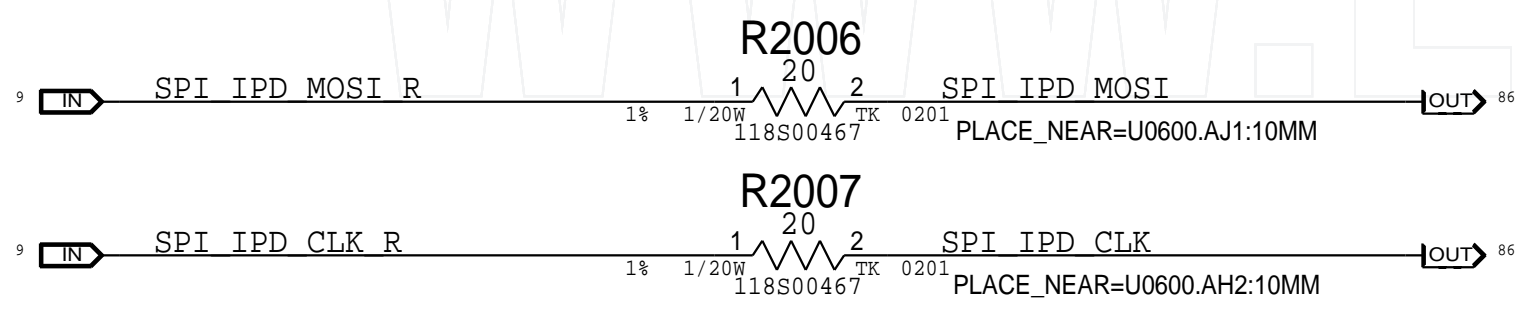
A SOC ROM Source Terminations



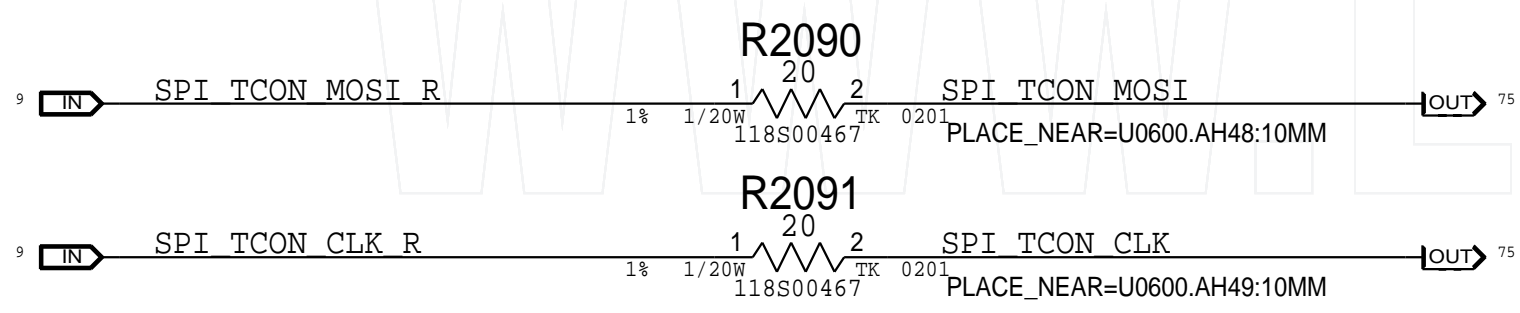
B TOUCHID Source Terminations



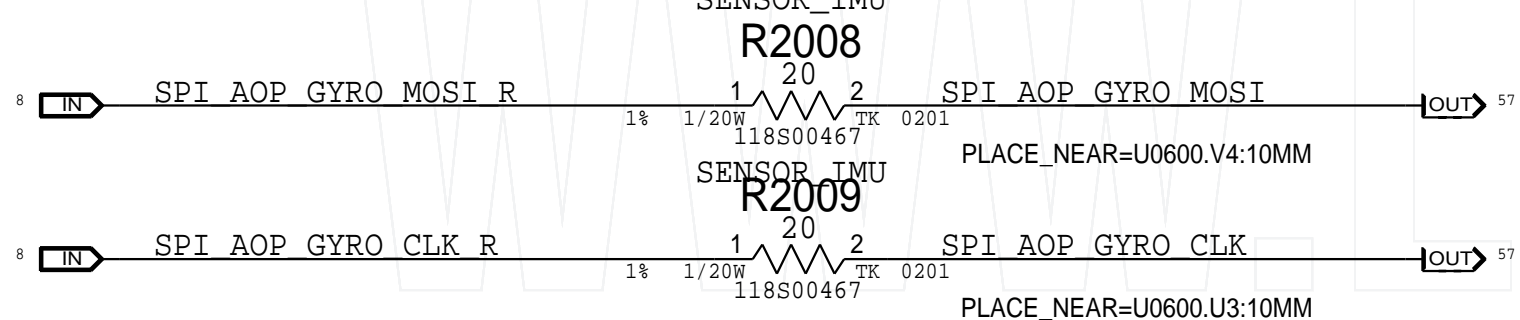
C IPD Source Terminations



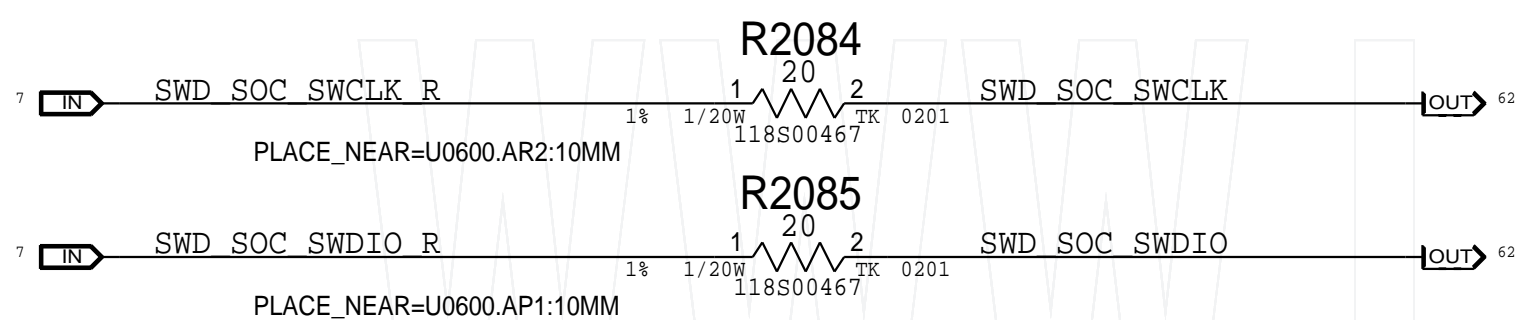
D TCON Source Terminations



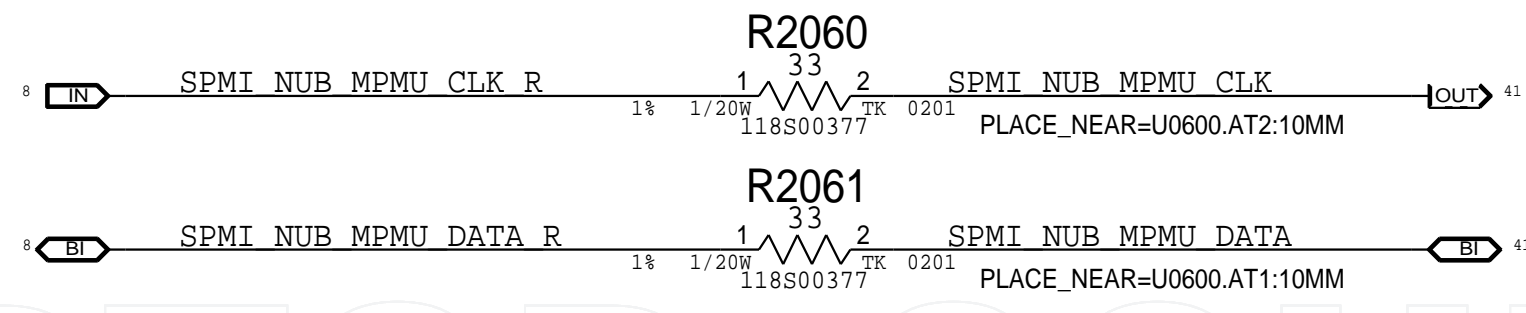
E IMU Source Terminations



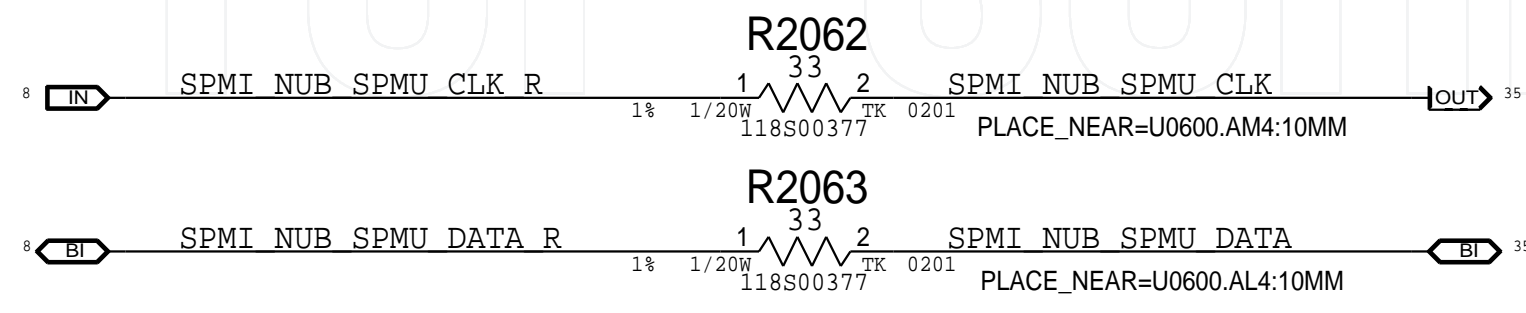
F SOC SWD Source Terminations



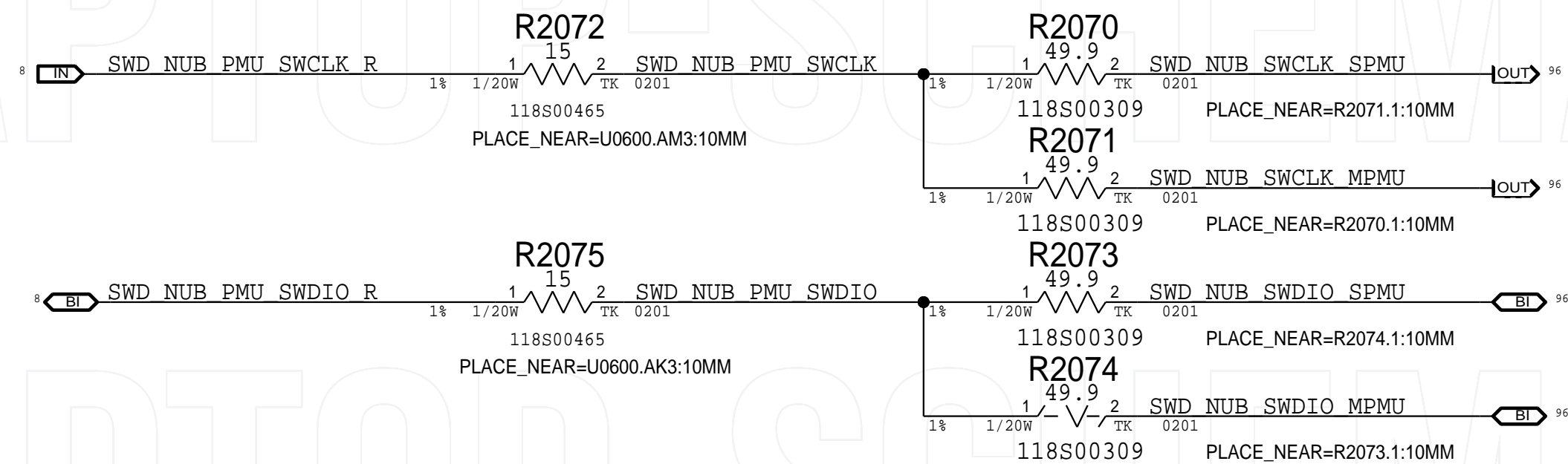
G SOC SPMI MPMU Source Terminations



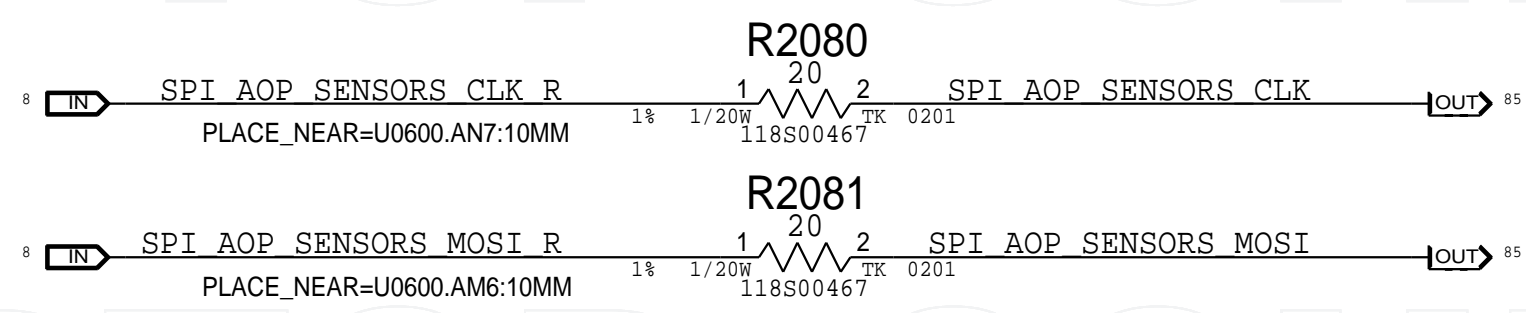
H SOC SPMI SPMU Source Terminations



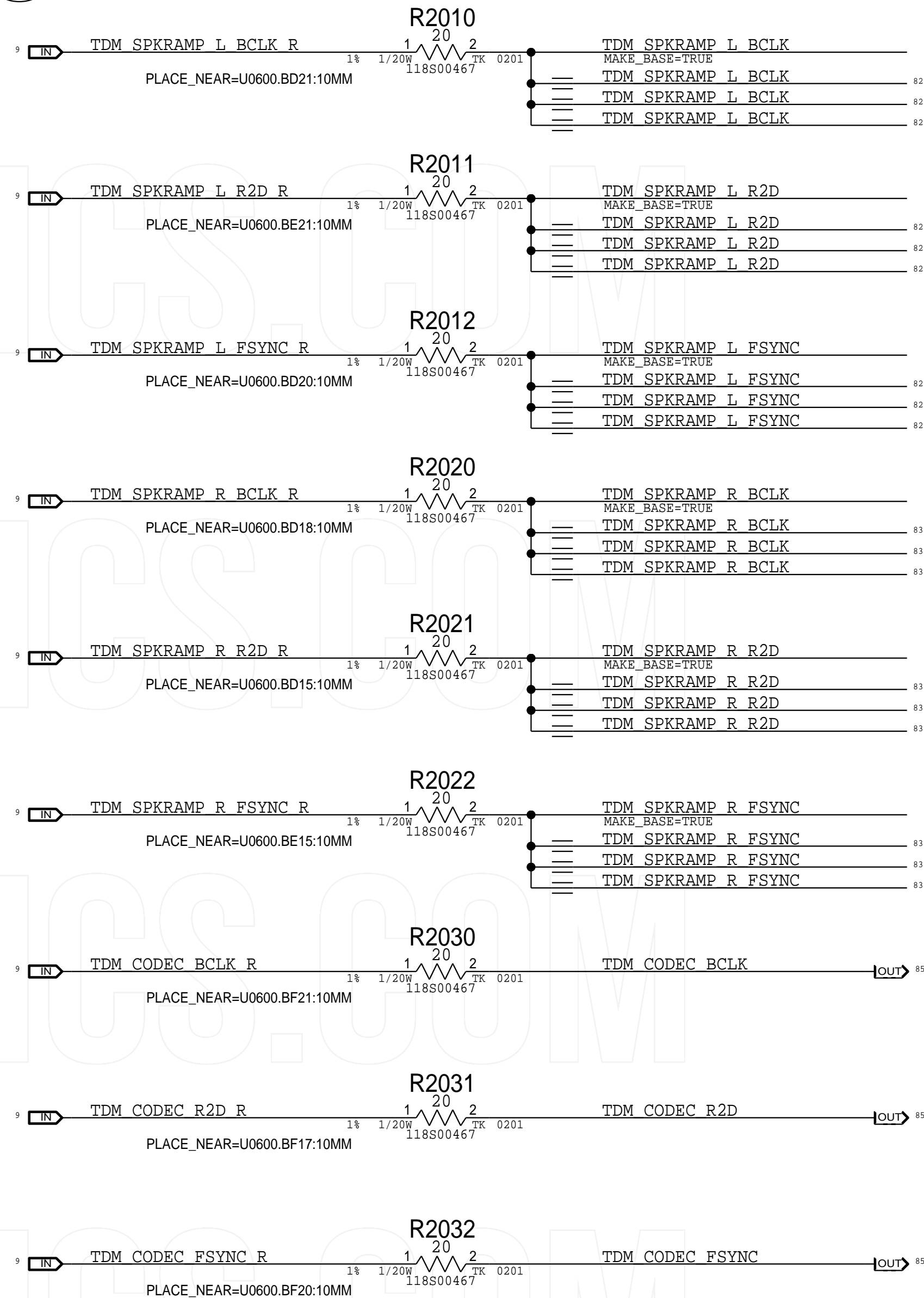
I PMU SWD Series R



J LAS Source Terminations



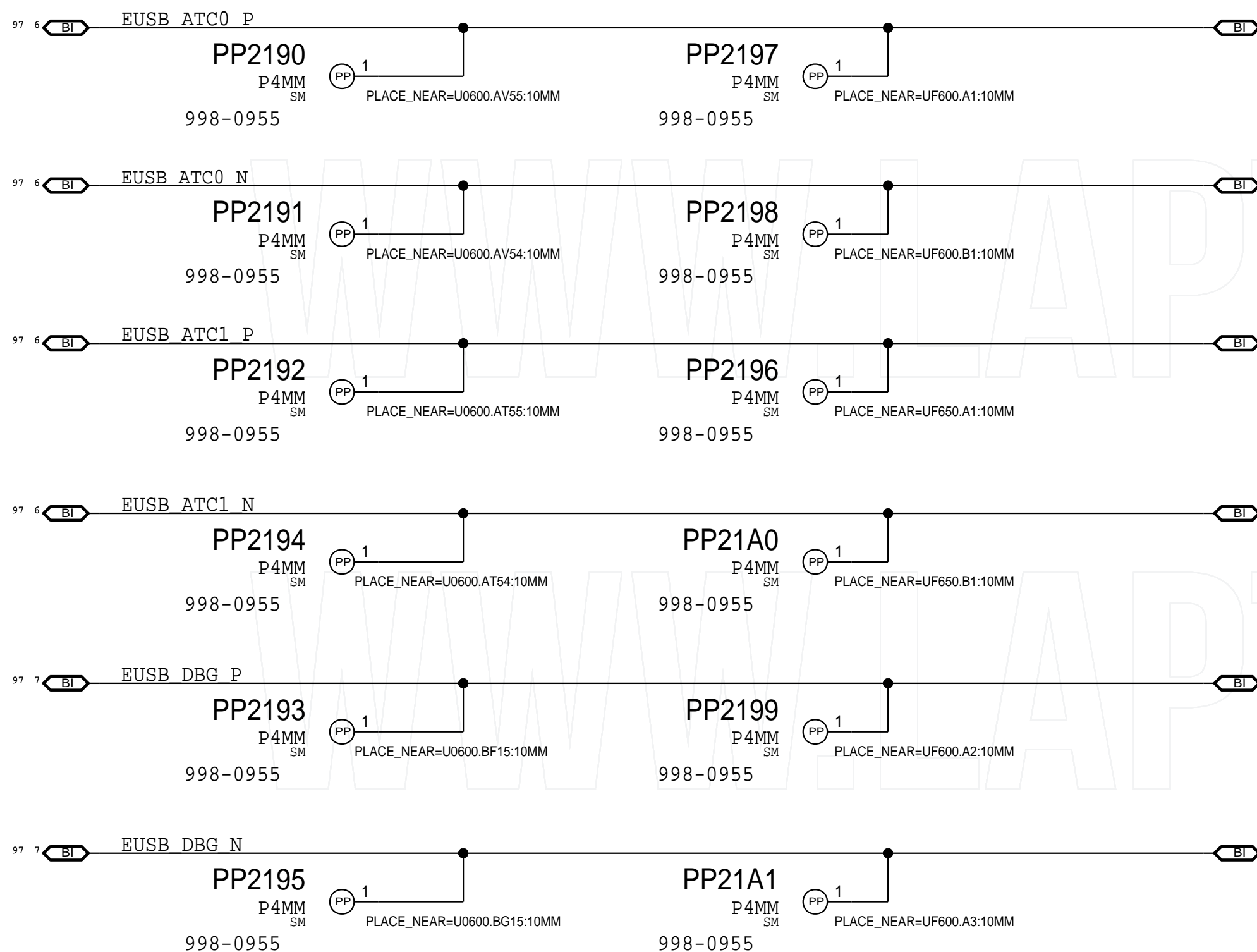
L TDM Source Terminations



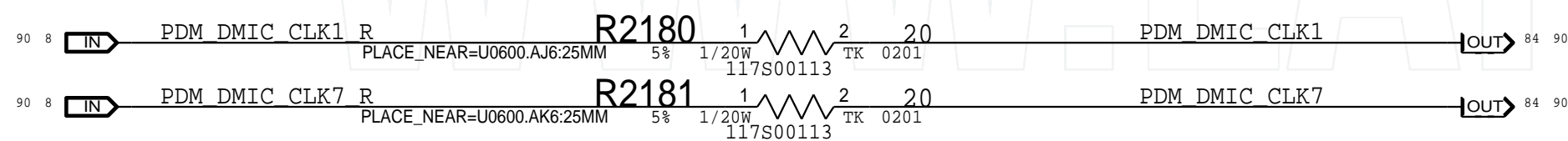
PAGE TITLE		
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BOM_COST_GROUP=SOC

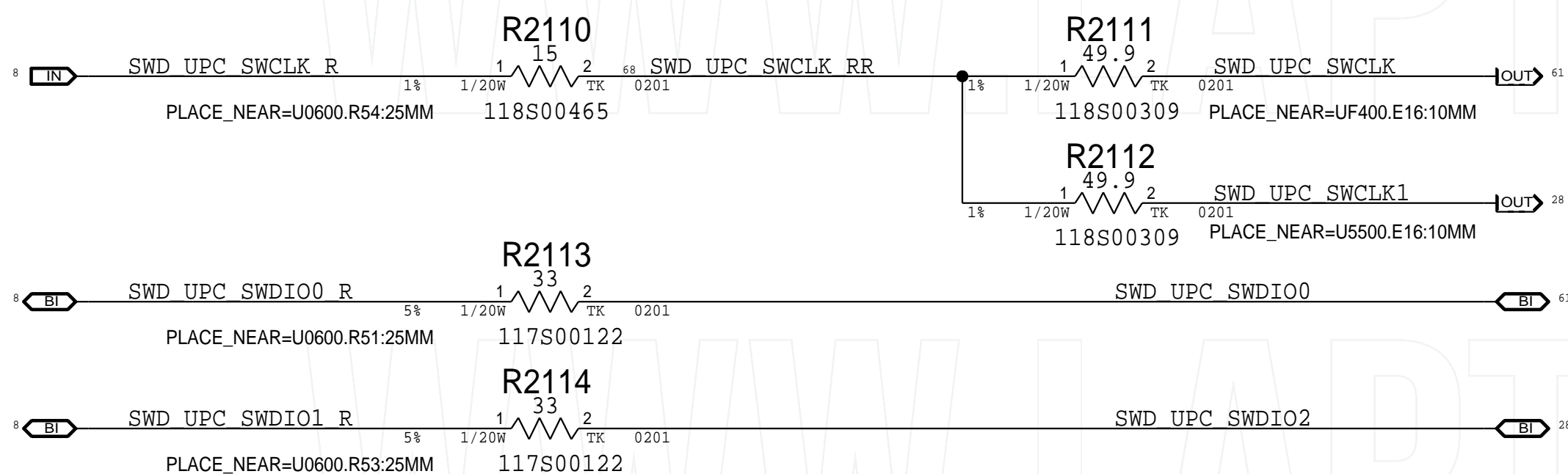
A EUSB Series Resistors & Test Points



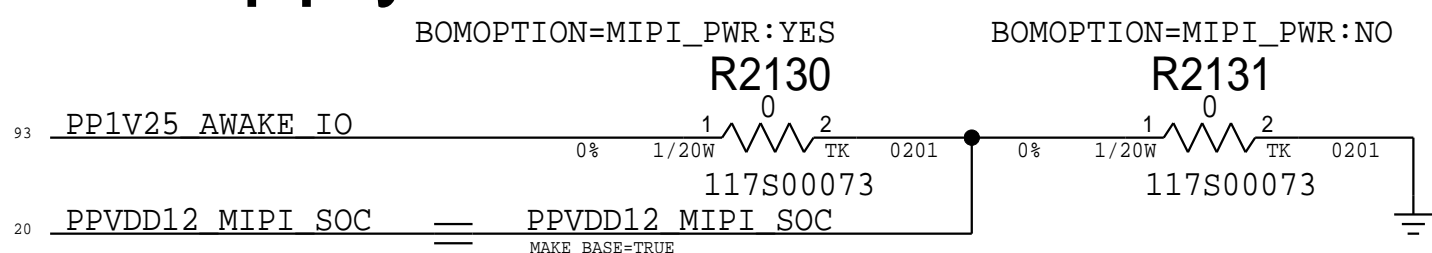
B DMIC Source Term



C UPC SWD Source Term

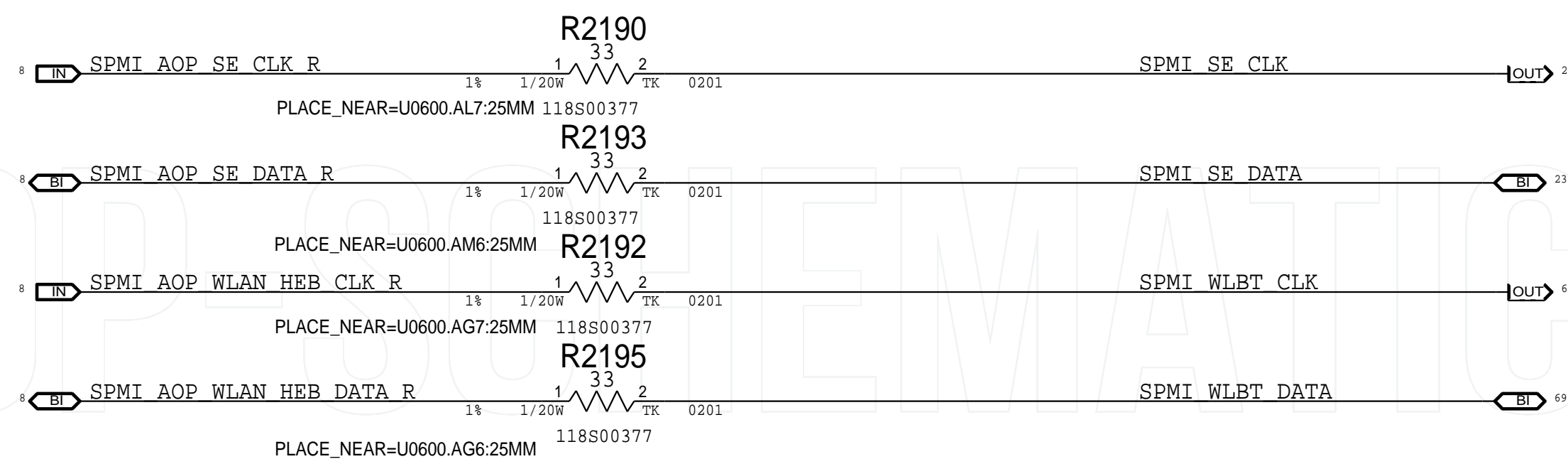


D MIPI PPVDD12 Supply Select

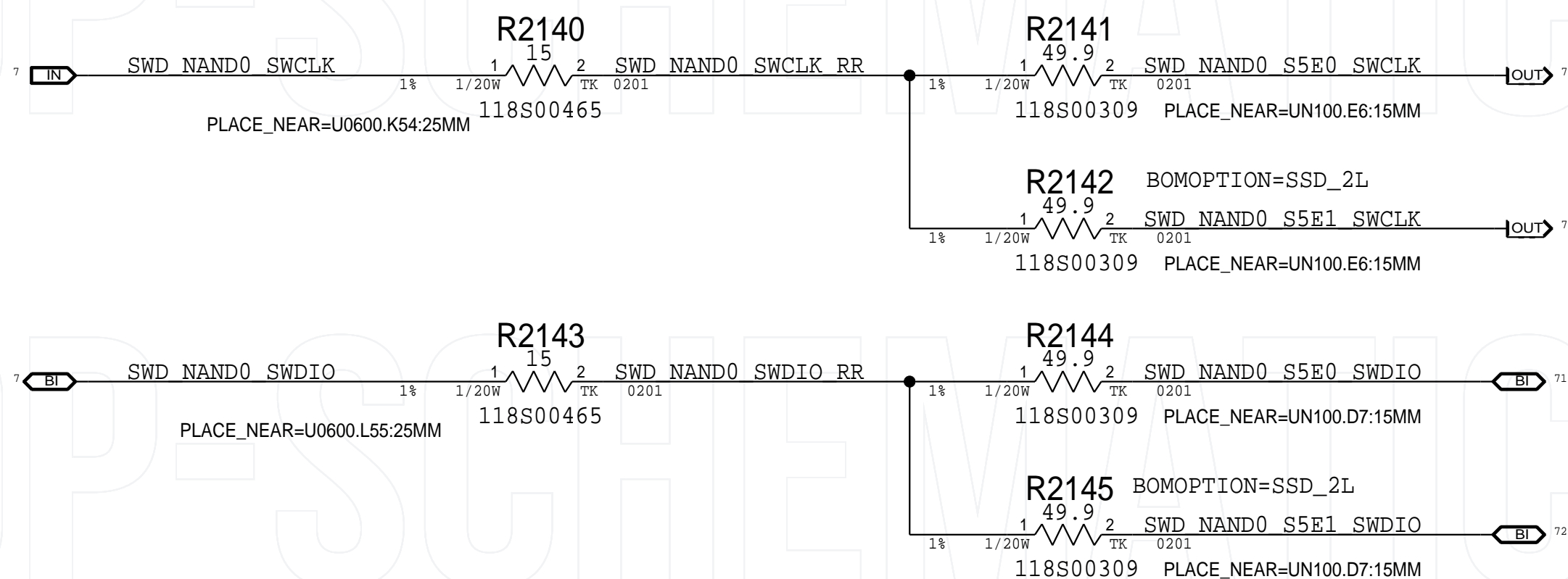


X2203 does not use the MIPI Interface on the SOC Interface
Per Moon Jung Kim (SEG Analog), VDD12_MIPIC and VDD12_MIPID can be tied to GND.

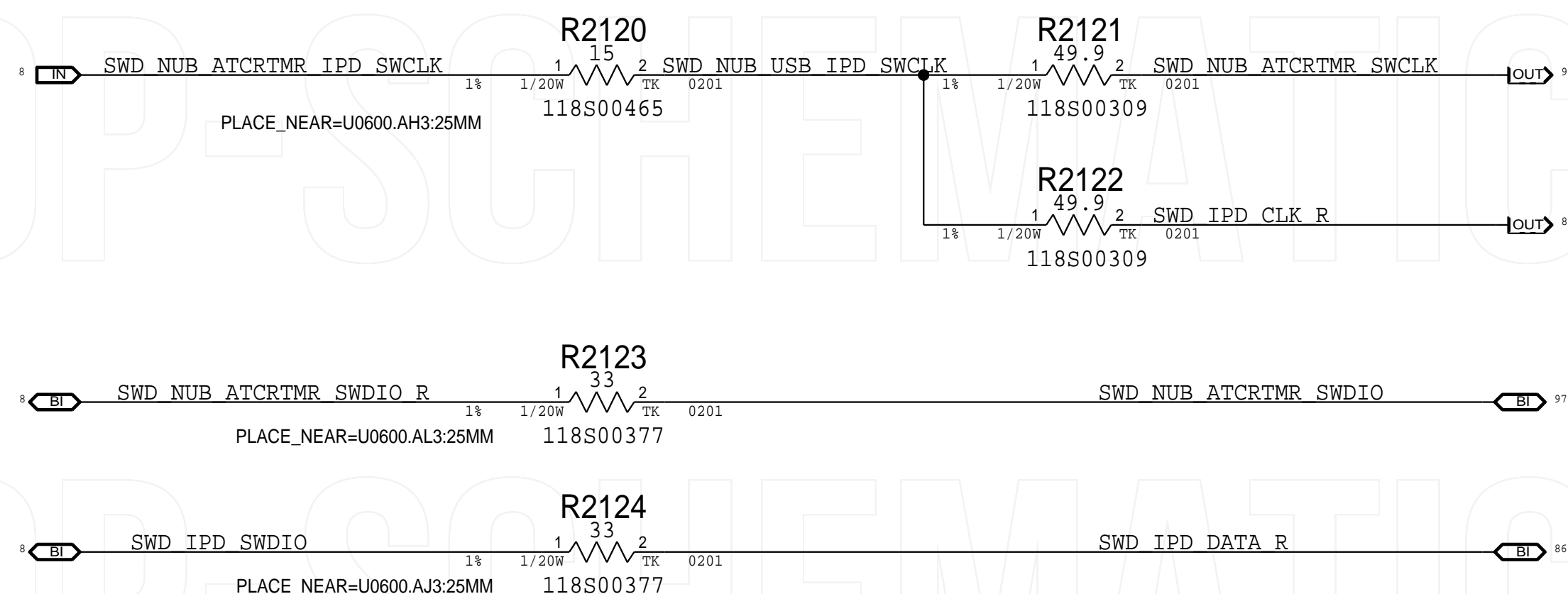
E Secure Element and WiFi SPMU Source Term



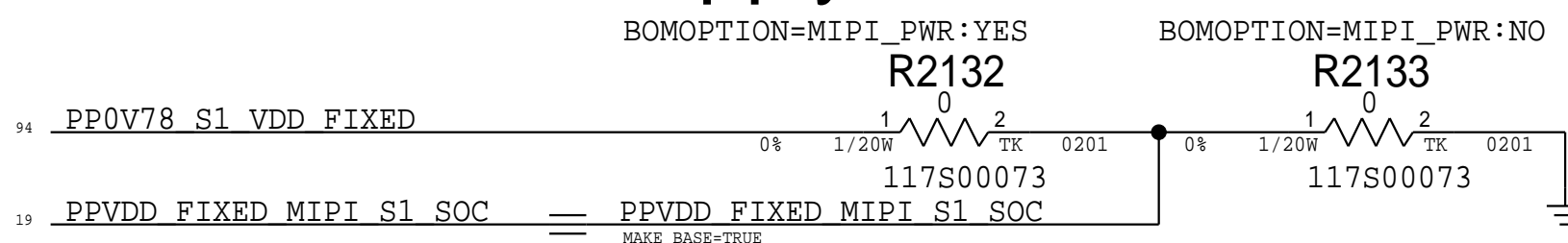
F NAND SWD Source Term



G IPD and ATC SWD Source Term

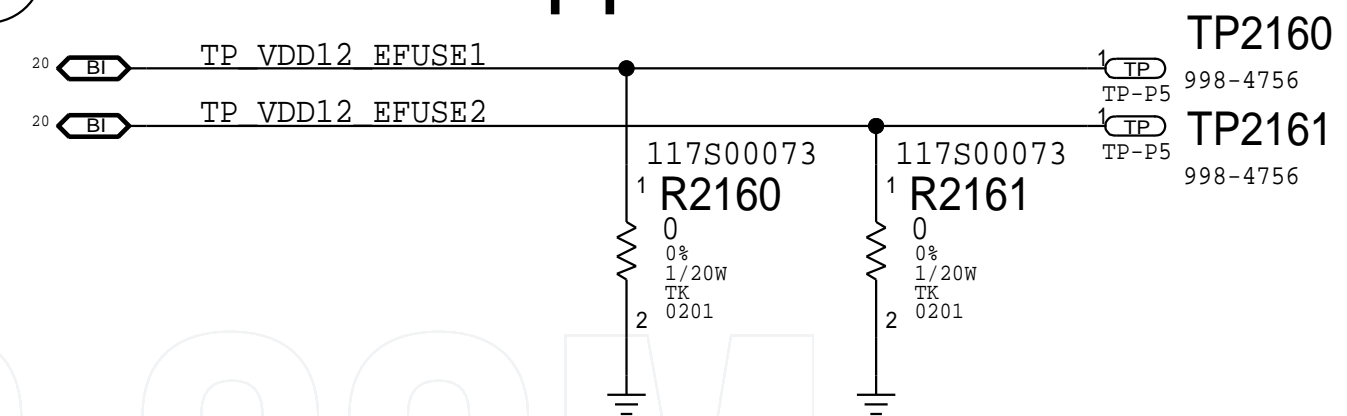


H MIPI PPVDD_FIXED S1 Supply Select



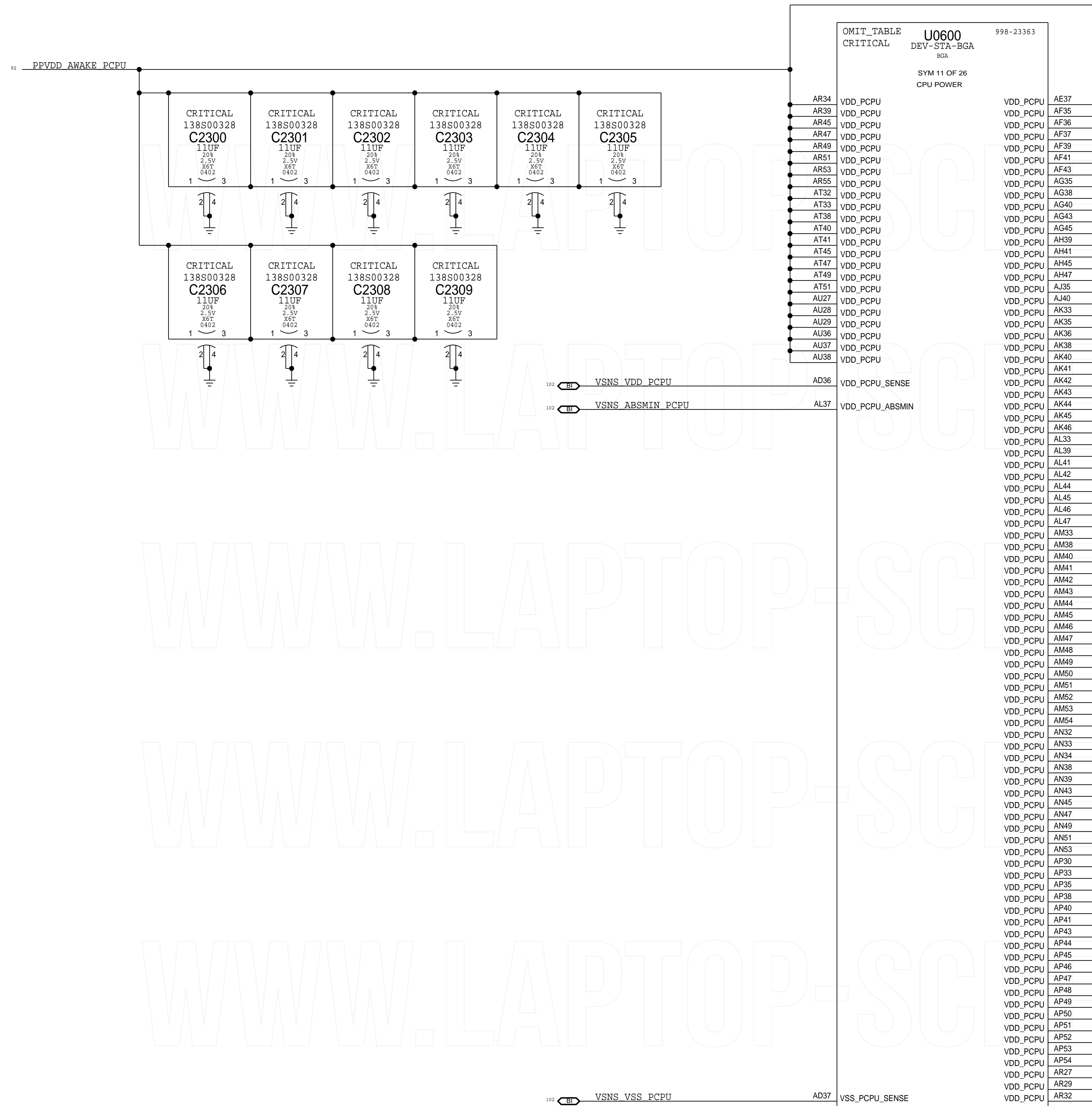
X2203 does not use the MIPI Interface on the SOC Interface
Per Moon Jung Kim (SEG Analog), VDD_FIXED_MIPIC_S1, VDD_FIXED_MIPID_PLL_S1, and VDD_FIXED_MIPID_S1 can be tied to GND.


I EFUSE Support



PAGE TITLE		
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	DRAWING NUMBER	051-07020
	REVISION	6.0.0
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SINC_MASTER=SOC		SINC_DATE=10/01/2021	
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		PAGE 23 OF 801	
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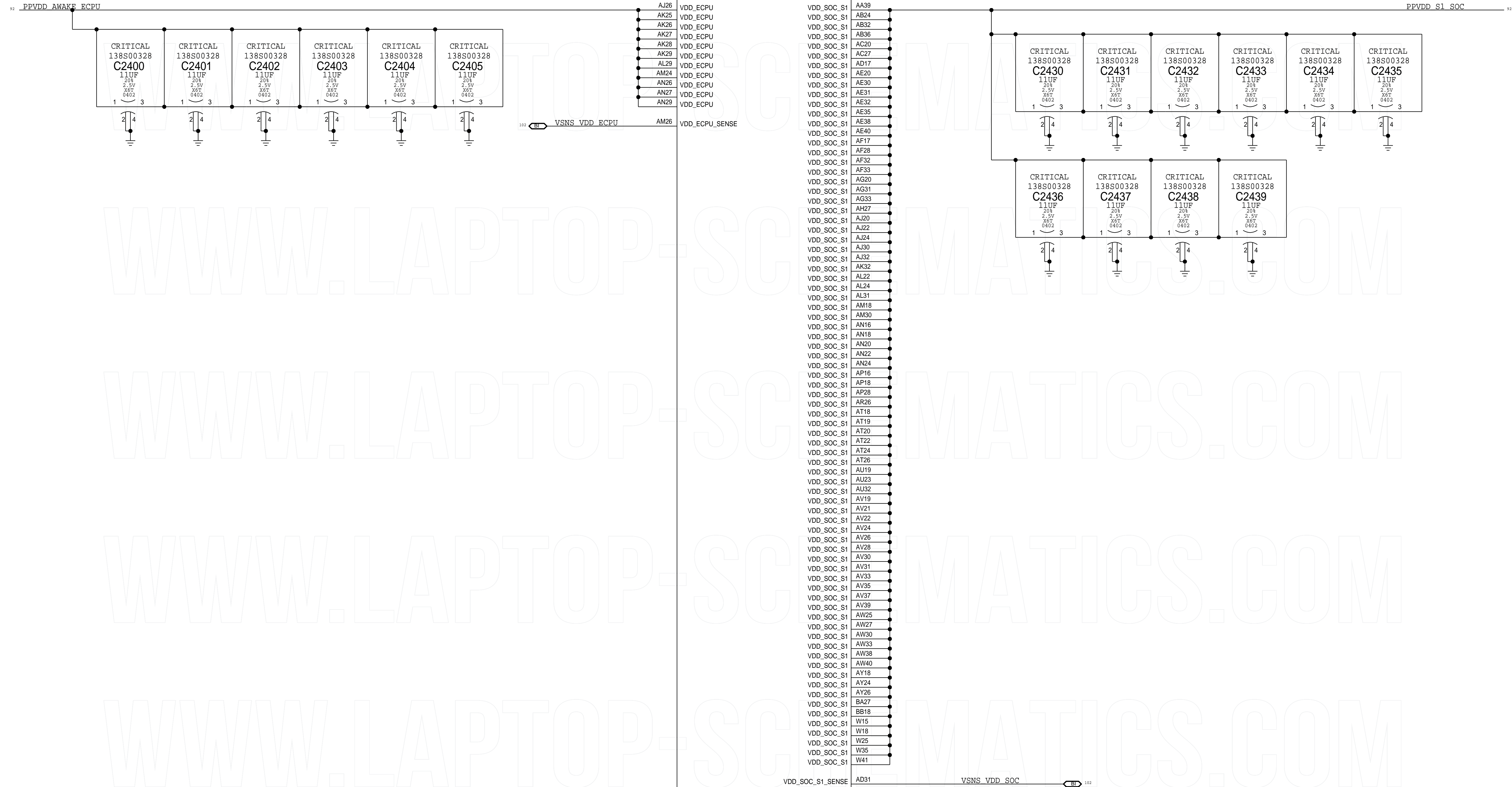
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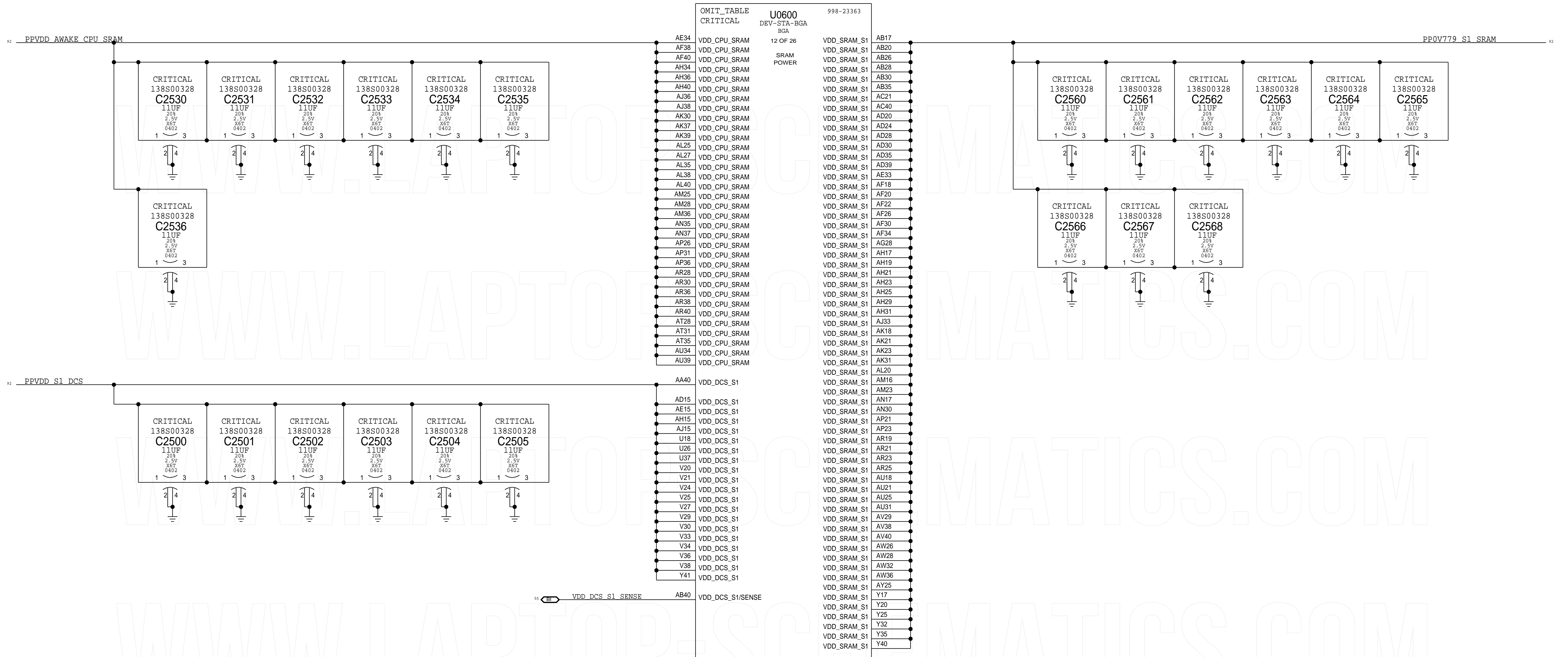
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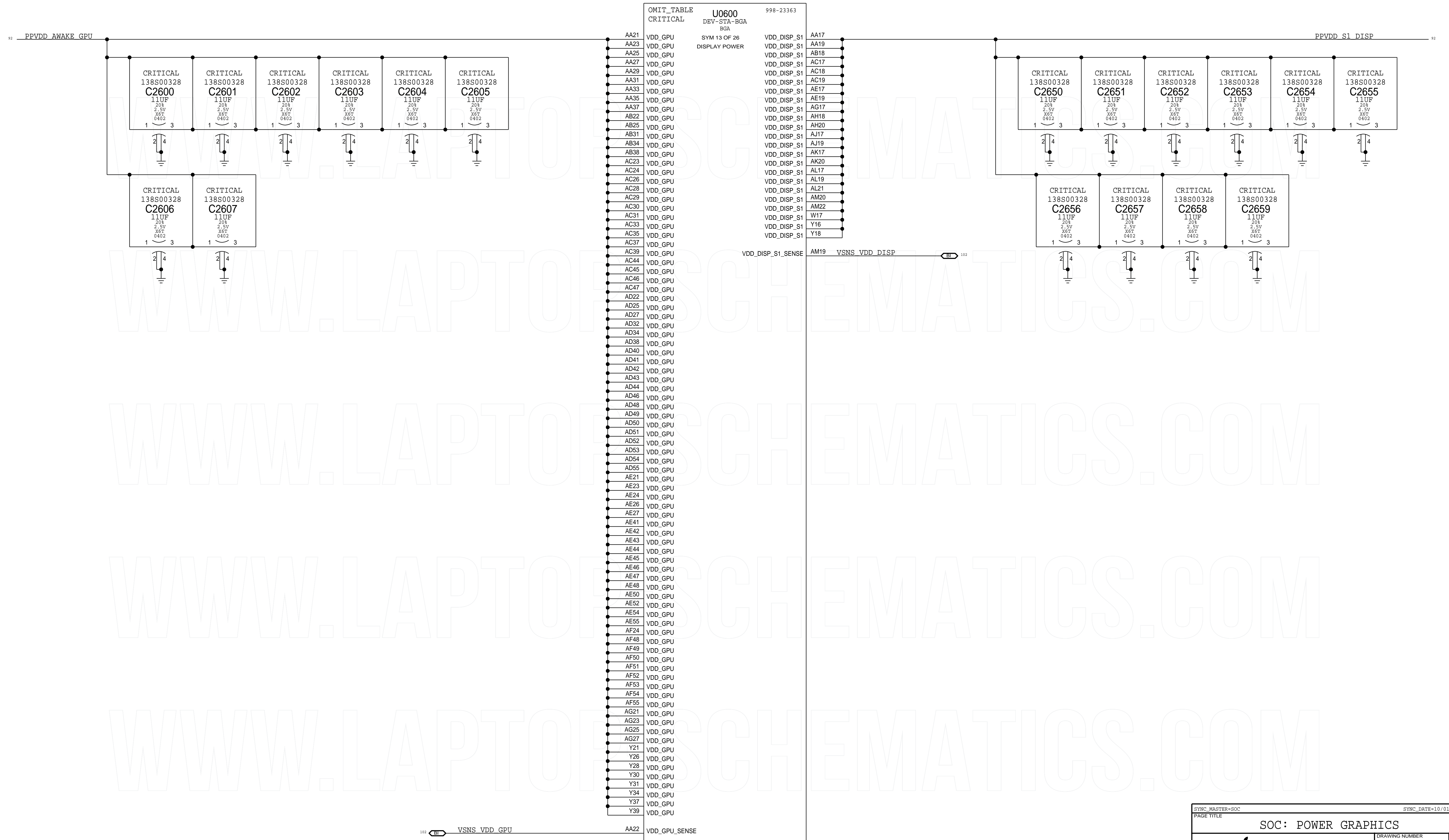


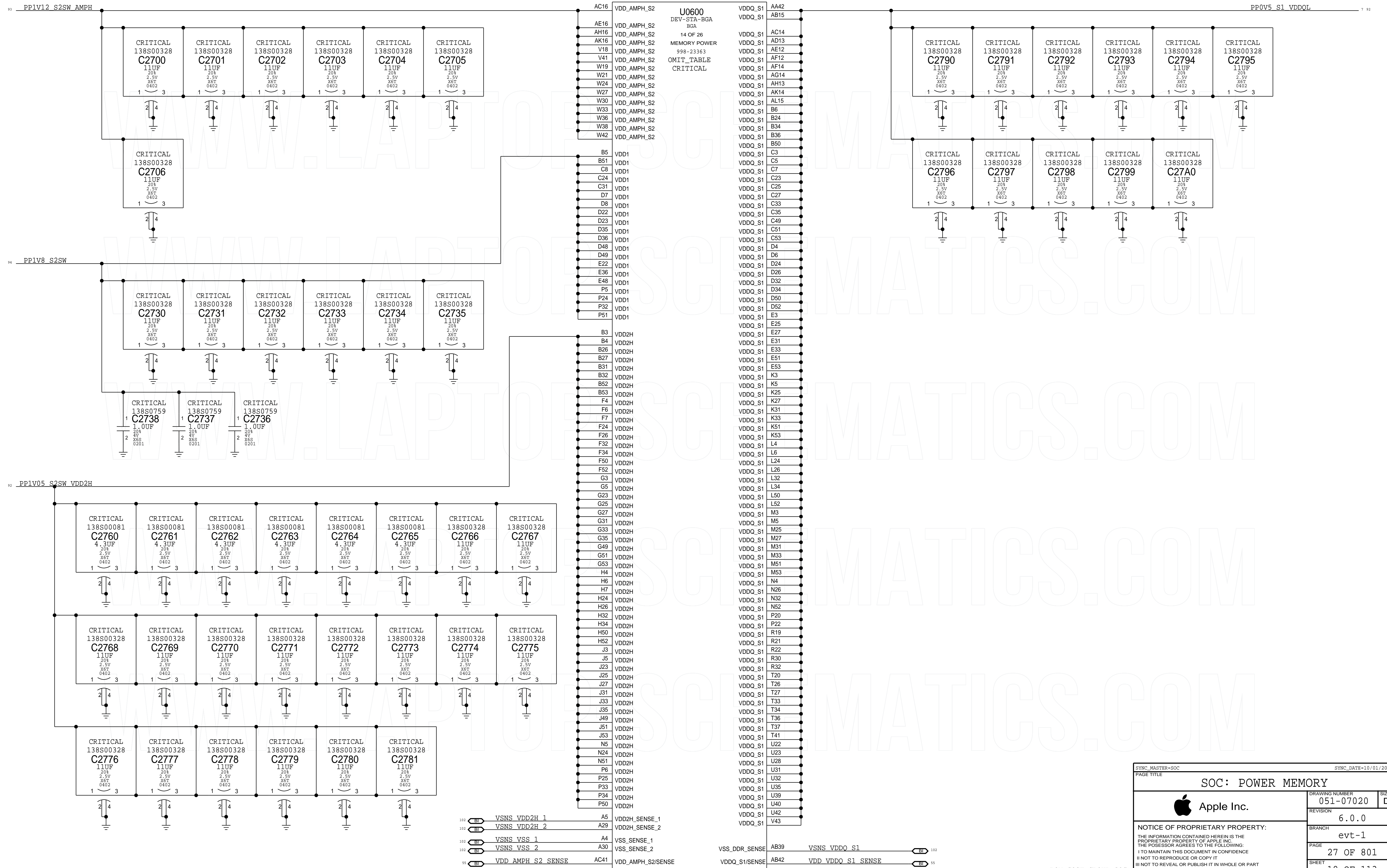
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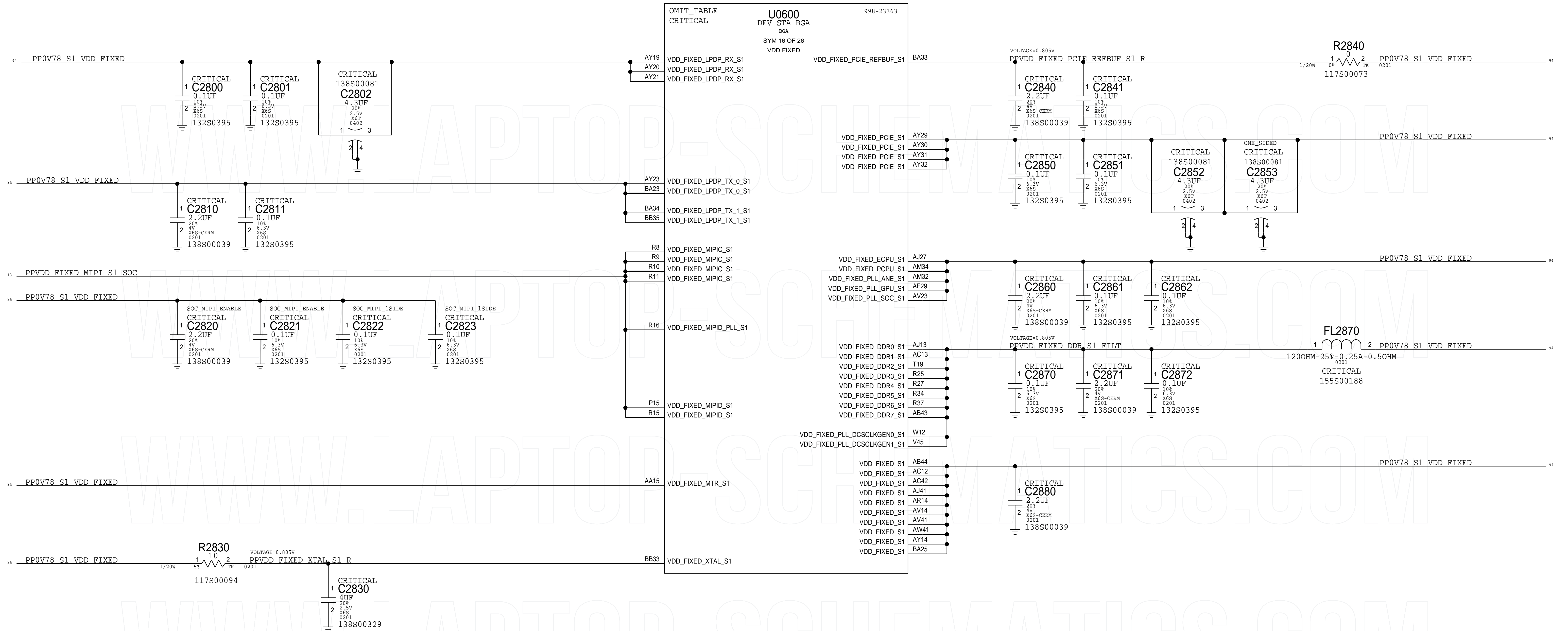
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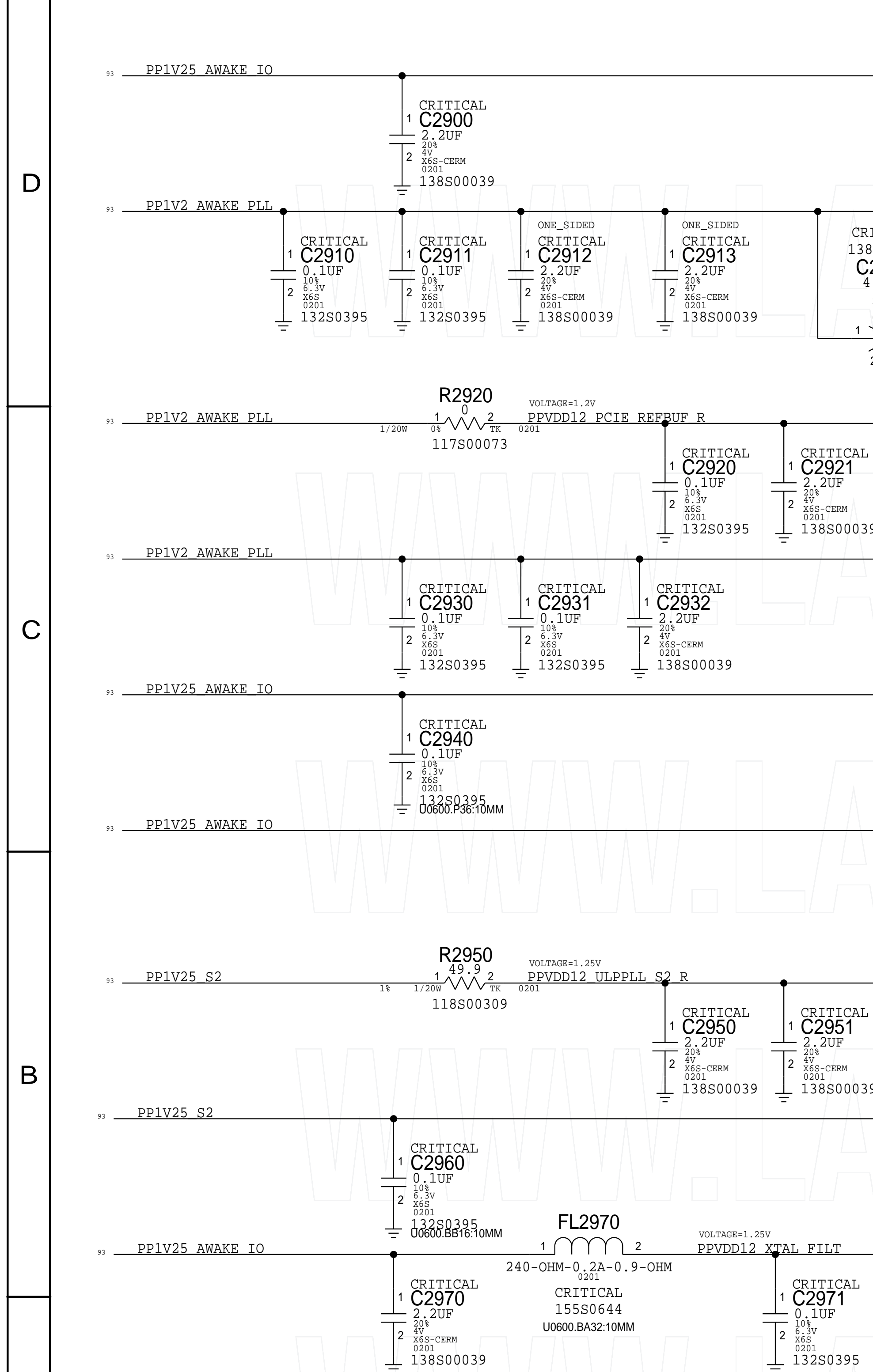
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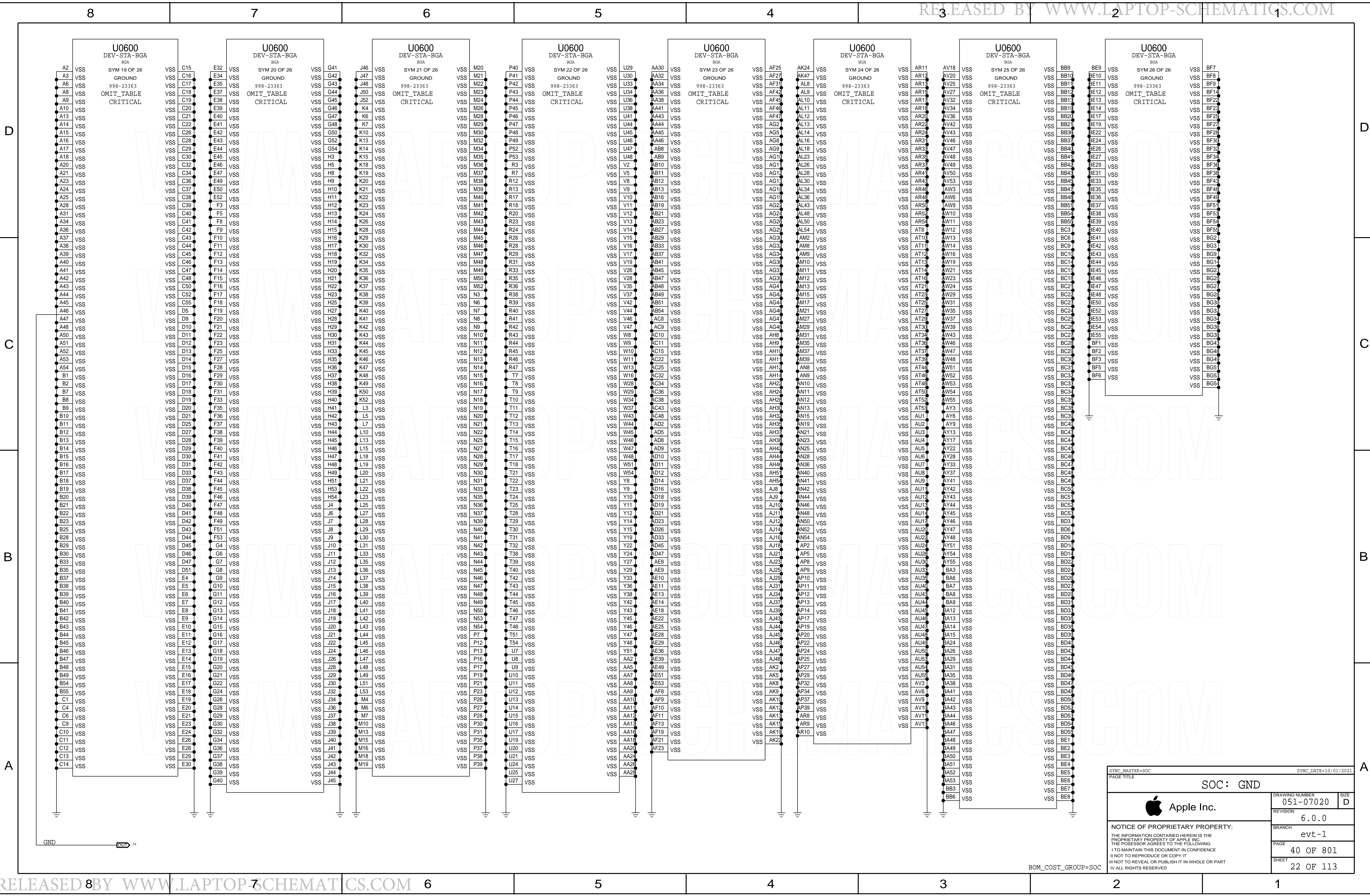




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SYNC_MASTER=SOC		SYNC_DATE=10/01/2021	
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		DRAWING NUMBER	051-07020
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BOM_COST_GROUP=SOC

Ceres - Secure Element

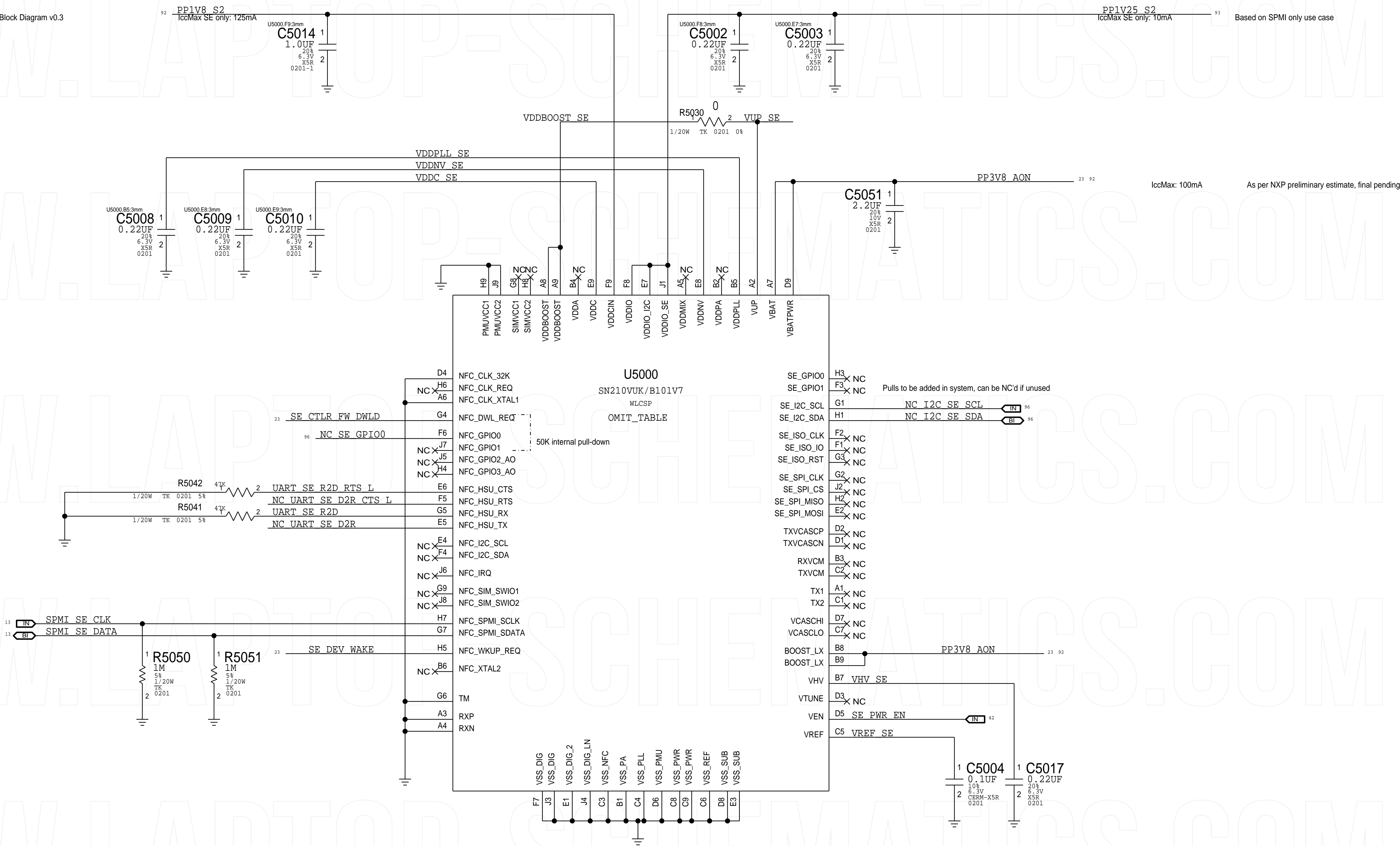
*** OK2INTEGRATE ***

Timing Requirements:
- VBAT supply ramp time: 20ms

Per TGA Power Block Diagram v0.3


Based on SPMI only use case

IccMax: 100mA As per NXP preliminary estimate, final pending

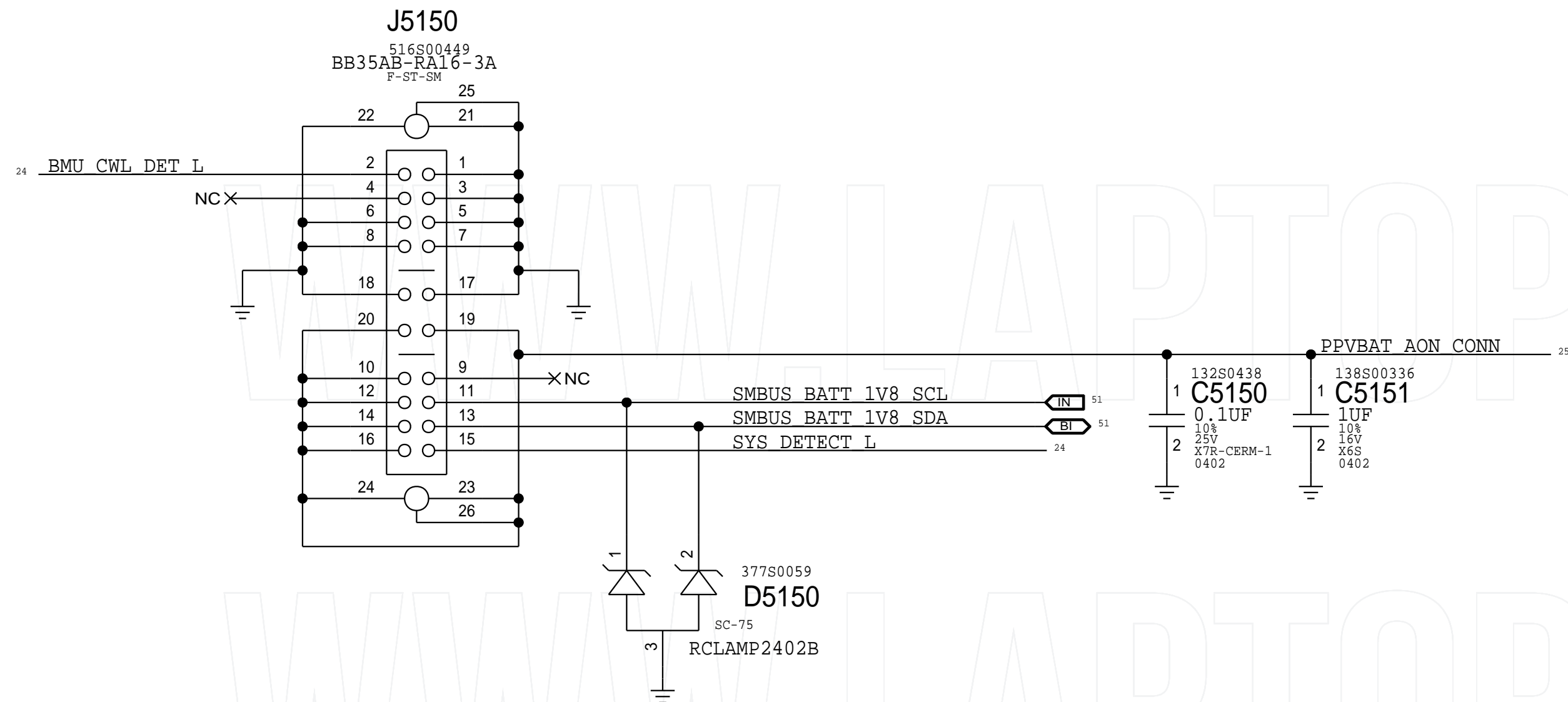


<rdar://problem/52067756> [SN200V] Wired Mode SE Only Reference Design Material
<rdar://problem/45108950> Mac - Venus Reference guide and De-coupling requirements

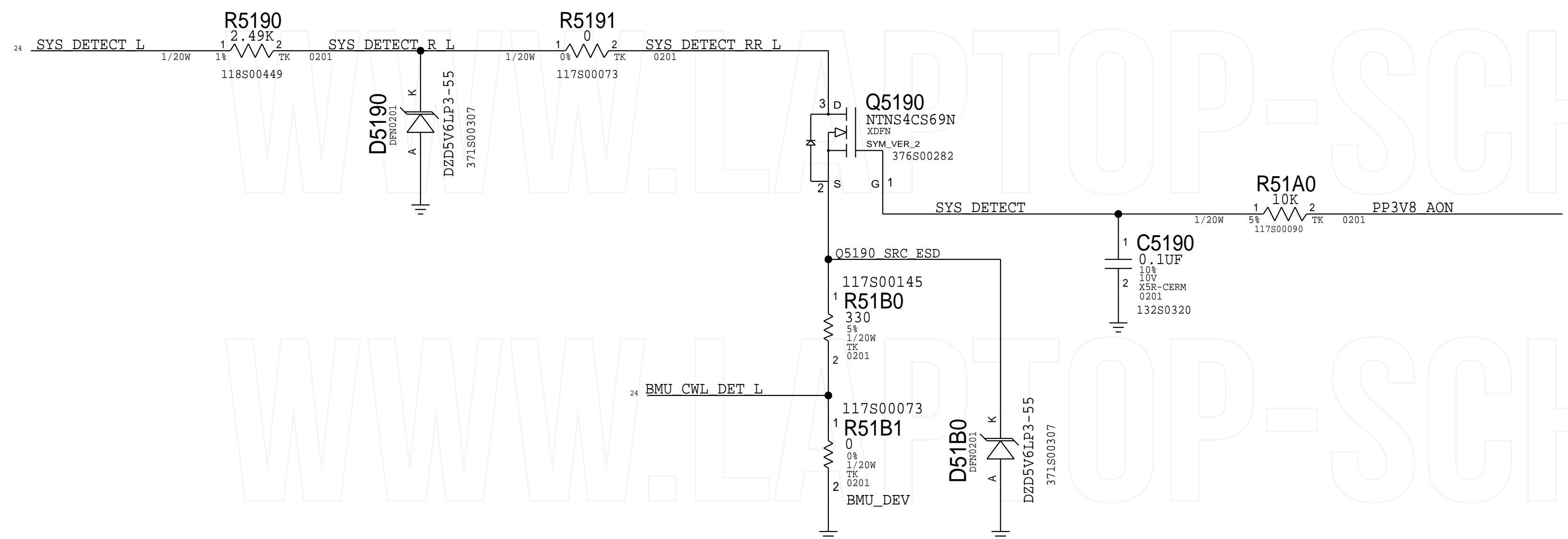
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PAGE TITLE		
Secure Element		
 Apple Inc.	DRAWING NUMBER	051-07020
	REVISION	6.0.0
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A BMU Connector



⑧ BMU SYS_DETECT Circuit



© BMU SYS_DETECT NOTES

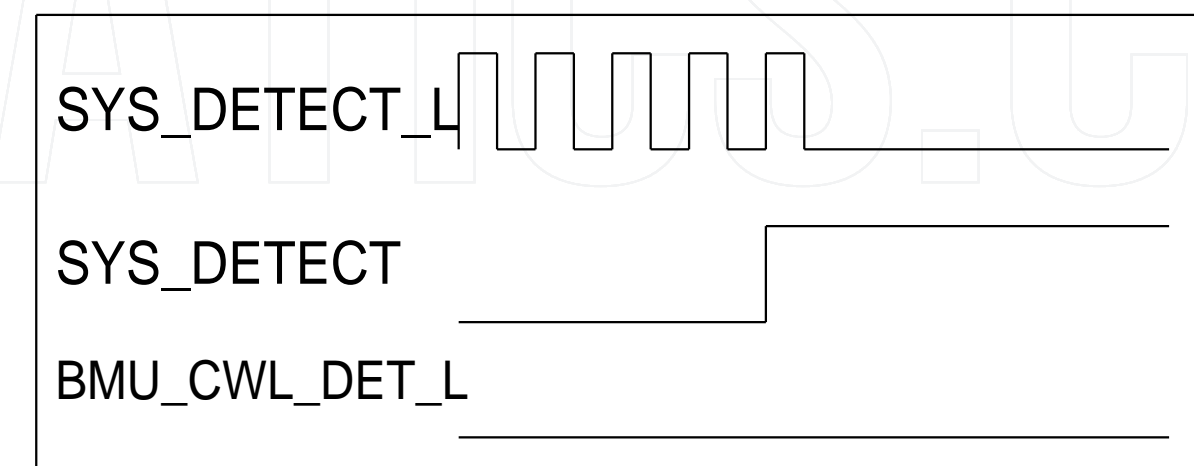
The BMU SYS_DETECT circuit relies on the system assembly in order to be properly enabled. During assembly, a metal gasket is placed between the cowling and the top-side of the BMU flex. The gasket is used to connect the BMU_CWL_DET_L signal, located between J5150.1 and Q5190.2, to GND. Once BMU_CWL_DET_L is tied to GND, then the SYS_DETECT circuit is ready to be enabled.

The BMU VBAT output will be enabled after the BMU flex and cowling are installed and power is supplied by connecting a power adapter to either the USB-C or MagSafe Connectors.


Thus the MLB remains in an unpowered state during system assembly.

Once the MLB is assembled into an enclosure, the BMU SYS_DETECT circuit output, SYS_DETECT_L, is continuously sampled by the Gas Gauge IC at a rate of once per second until it detects a logic low. During the once per second interval, an internal pull-up within the Gas Gauge IC is enabled for 4us to conserve battery charge. Once a logic low is detected, then the BMU enables the VBAT output voltage.

Below is an example waveform showing how the BMU SYS_DETECT circuit works.



In the event that the cowlings needs to be removed while retaining power to the MLB, resistor R51B1 can be loaded.

PAGE NUMBER		PAGE TOTALS	
PAGE TITLE			
BMU Connector			
 Apple Inc.	DRAWING NUMBER		SIZE D
	051-07020		
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	BRANCH		evt-1
	PAGE		51 OF 801
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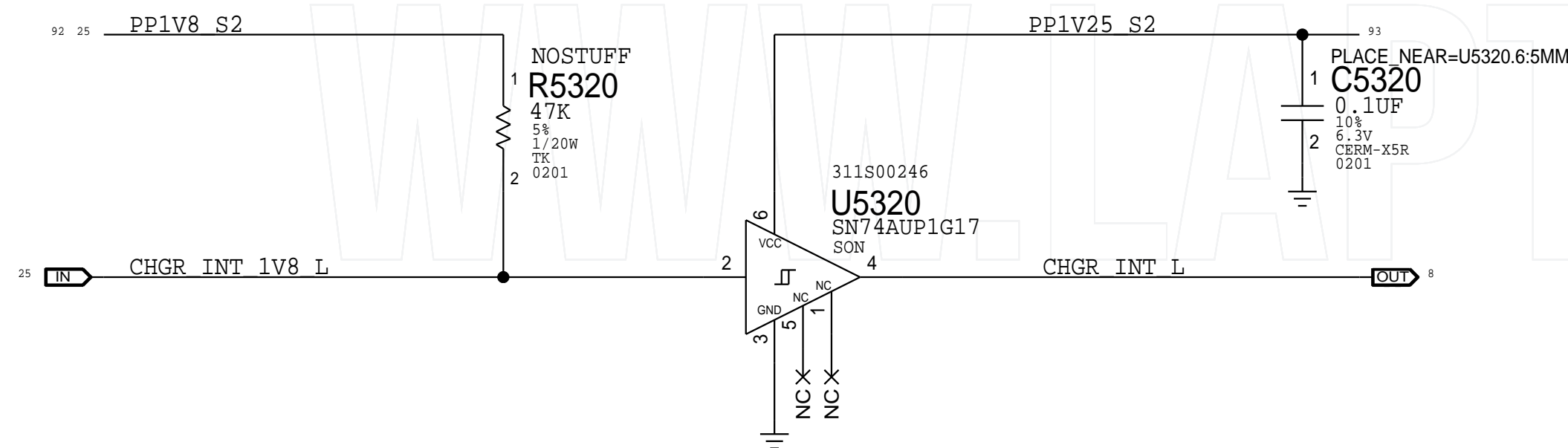
*** OK2INTEGRATE ***

CHGR I2C Level Translation

SMBUS_CHGR_1V8_[SCL/SDA]: Level translation circuit to be placed in project specific I2C page.

CHGR_INT_L Level Translation

Stuff R5320 in case, glitch during power sequencing is a concern.

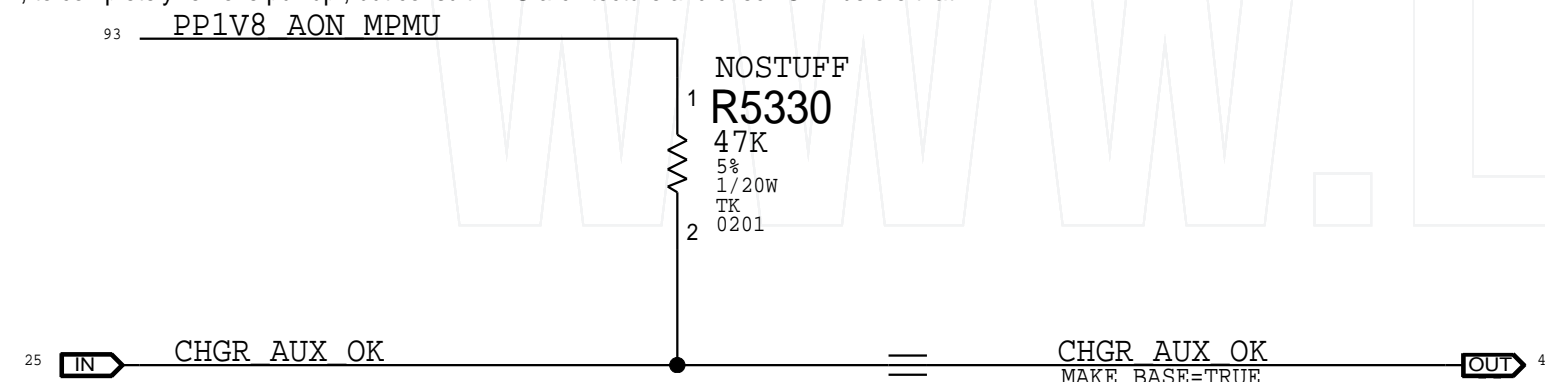


CHGR_AUX_OK Pull Up

Pull up to MPMU LDO9, or rely on MPMU internal pull up.

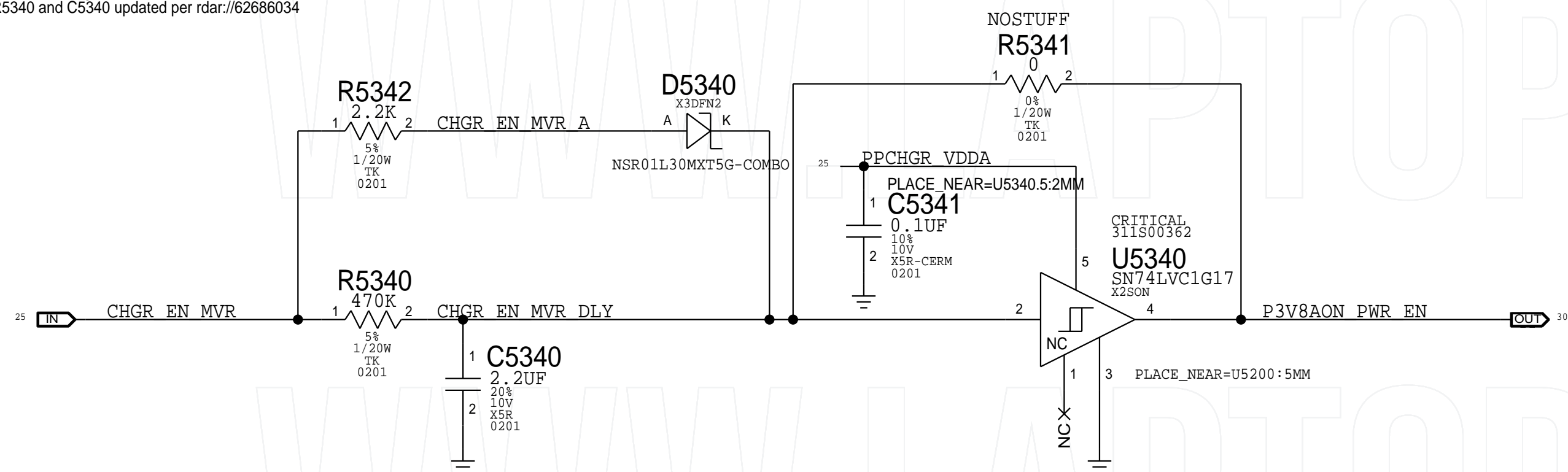
OK, to completely remove pull up , but consult PMU architecture and check OTP before that

OK, to completely remove pull up , but consult PMU architecture and check OTP before that

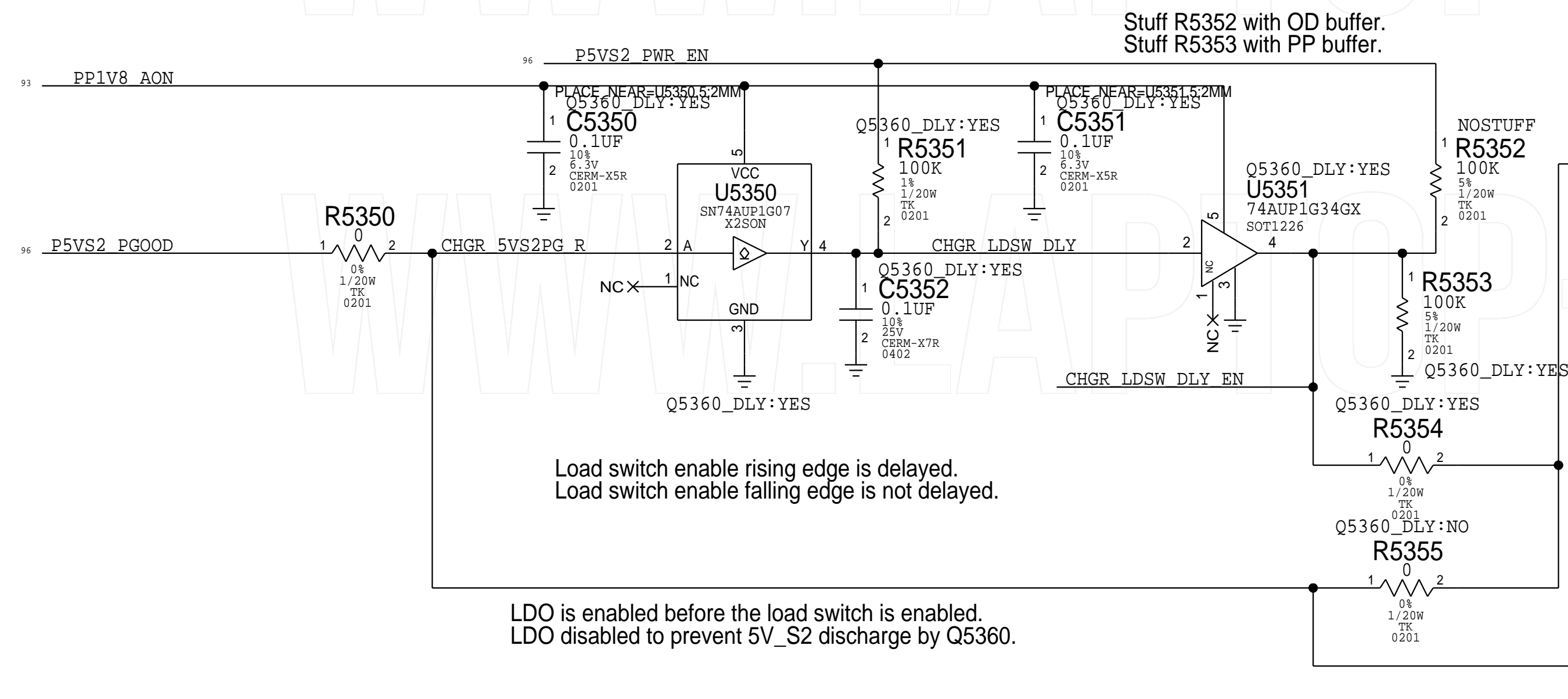


Delay for 3.8V VR Enable

R5340 and C5340 updated per rdar://62686034



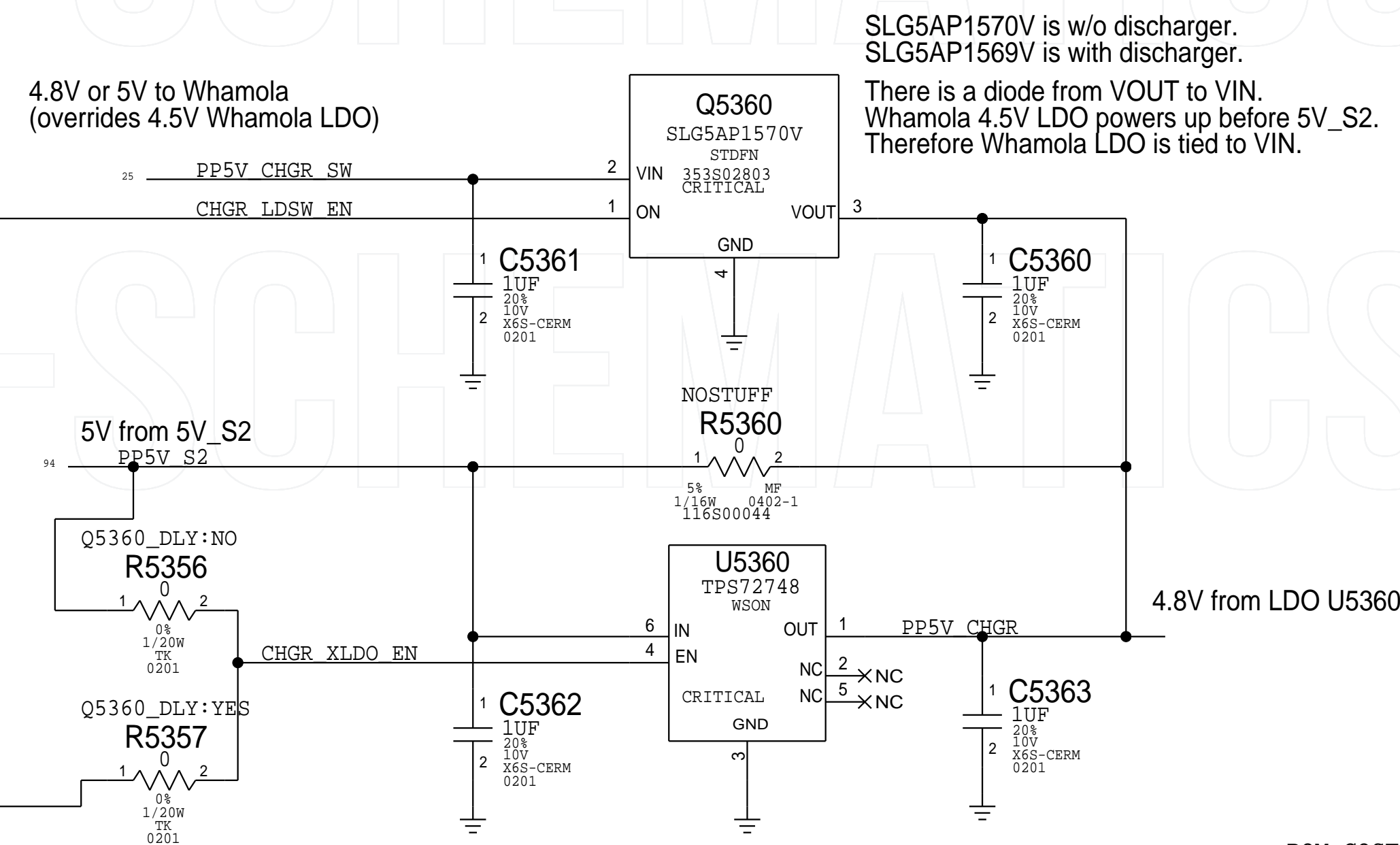
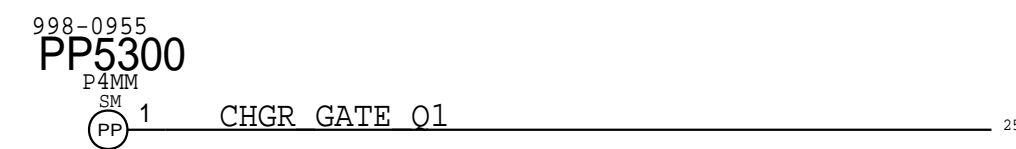
SWITCHOVER TO EXTERNAL 5V



Load switch enable rising edge is delayed.
Load switch enable falling edge is not delayed.

LDO is enabled before the load switch is enabled.
LDO disabled to prevent 5V_S2 discharge by Q5360.

Probe points - bottom



SI G5AP1570V is w/o discharger.

SLG5AP1569V is with discharger.


There is a diode from VOUT to VIN

There is a diode from VOUT to VIN

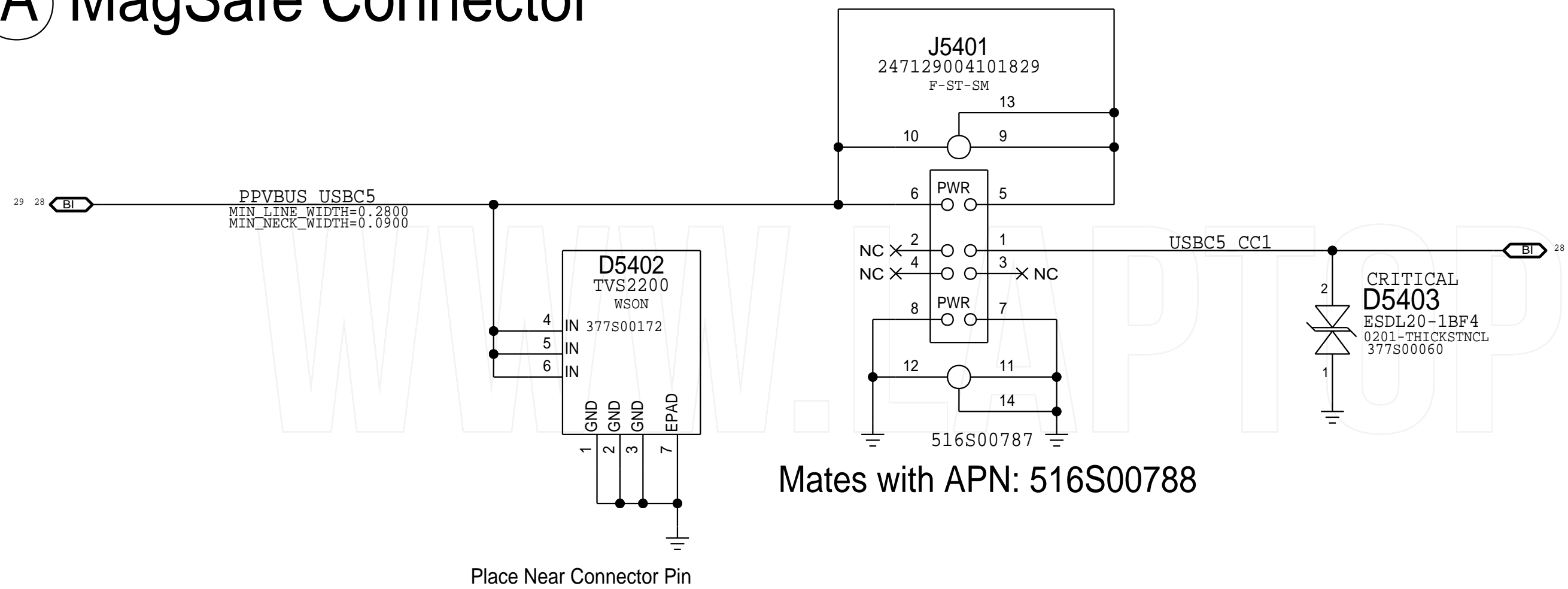
Whamola 4.5V LDO powers up before 5V. S2

Therefore Whamola LDO is tied to VIN.

Therefore Whamola EDC is tied to VIN.

FORM 200-10720-01 (04/04)		FORM 200-10720-01 (04/04)	
PAGE TITLE			
BATTERY CHARGER SUPPORT			
 Apple Inc.	DRAWING NUMBER 051-07020		SIZE D
	REVISION 6.0.0		
	BRANCH evt-1		
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A MagSafe Connector



PAGE TITLE		
MAGSAFE: CONNECTOR		
	DRAWING NUMBER	051-07020
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BOM_COST_GROUP=MAGSAFE

Either a Testpoint or Arkanoid connector must be present for GPIO0 (EVEN IN PRODUCTION)

D

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B

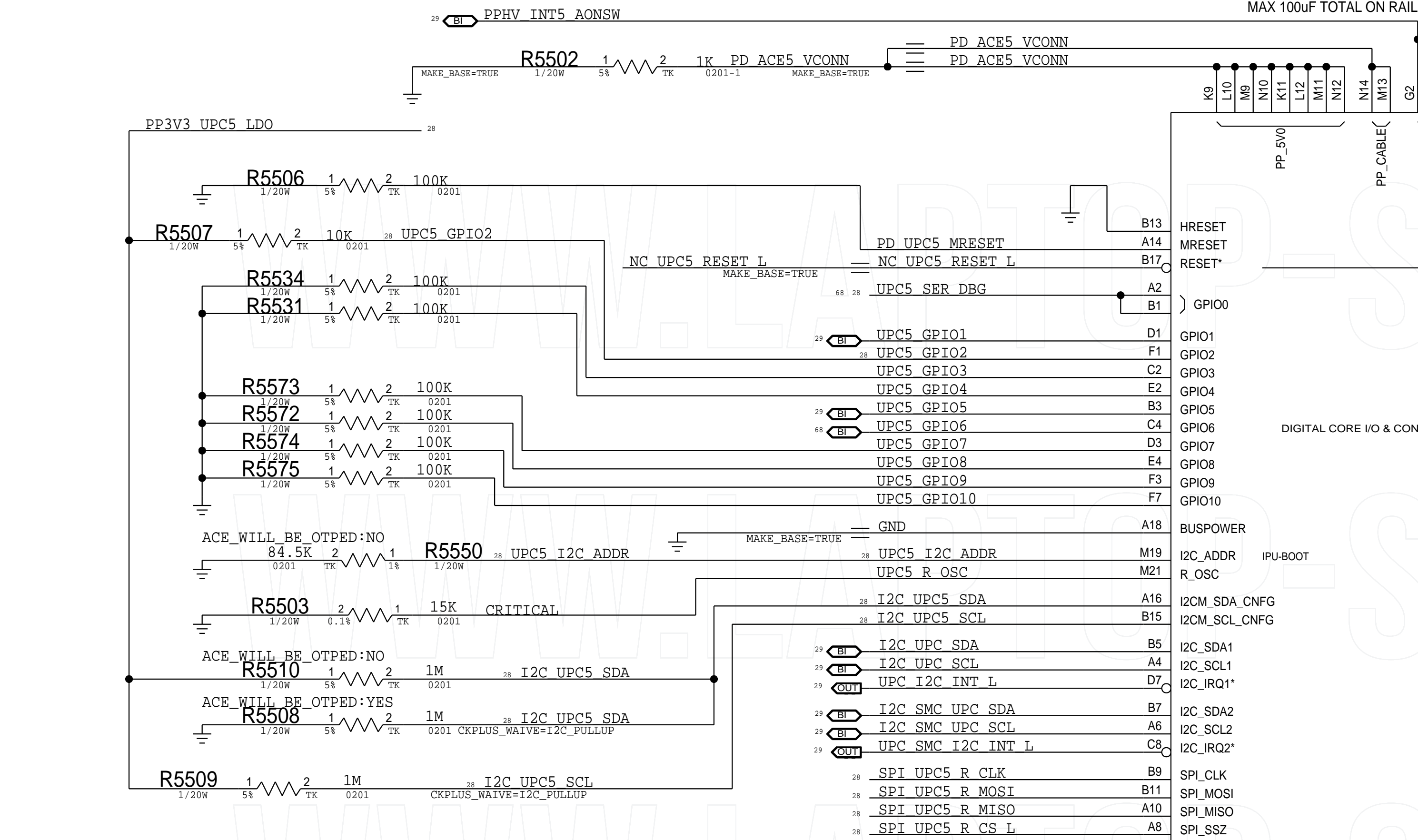
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Configured as UPC5 (the 6th slot)

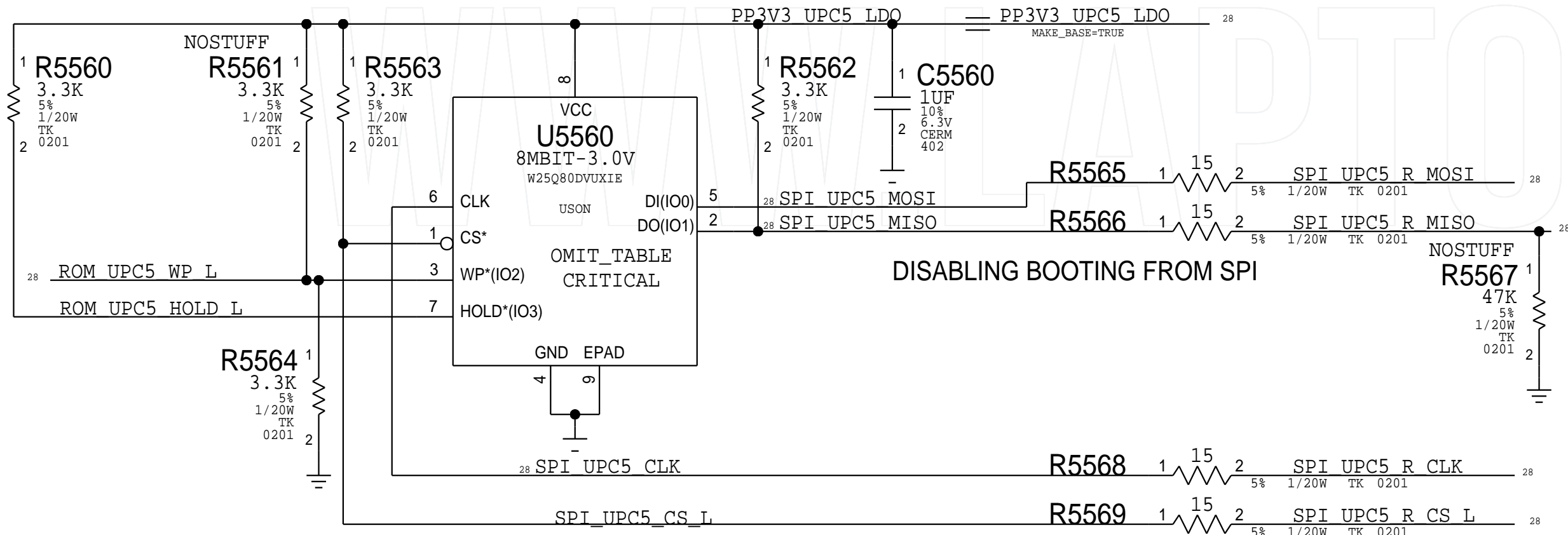
ACE_WILL_BE_OTPED:YES (POR)
If Ace can be OTPed
before installing bundle.
(ICT station is ready)

I2C_ADDR=Float
I2CM_SCL_CNFG=HIGH
I2CM_SDA_CNFG=LOW

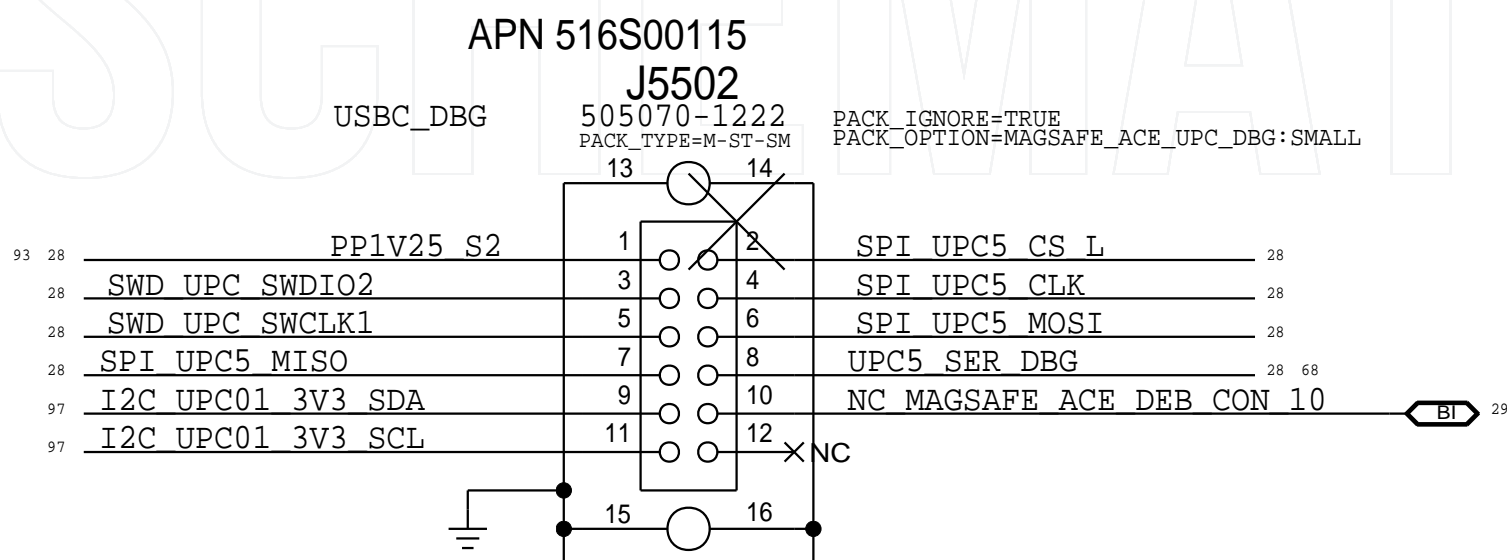
ACE_WILL_BE_OTPED:NO
Like in P0, Or EE bring up
Prevents I2C Conflict with
Other Aces before OTP

I2C_ADDR=84.5K PD
I2CM_SCL_CNFG=HIGH
I2CM_SDA_CNFG=HIGH

SPI ROM



AARDVARKANOID CONN



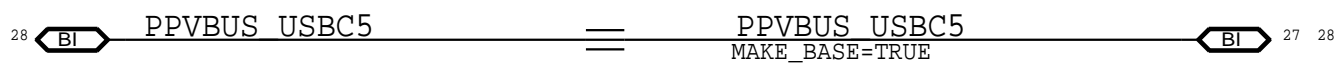
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MAGSAFE: PORT CONTROLLER		
	DRAWING NUMBER	051-07020
	REVISION	6.0.0
	BRANCH	evt-1
	PAGE	55 OF 801
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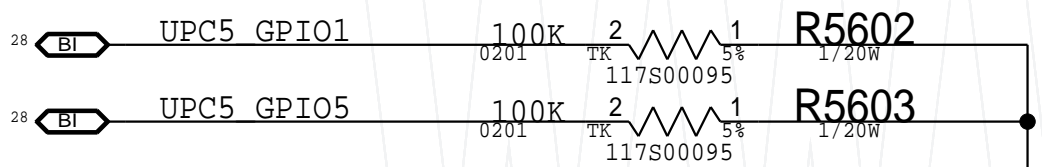
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A 20V Aliases

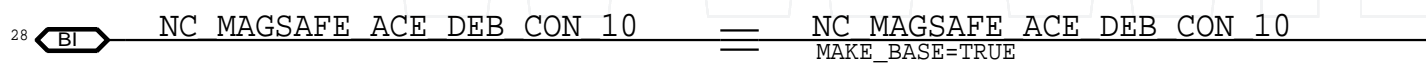
POWER ALIASES



GPIOs

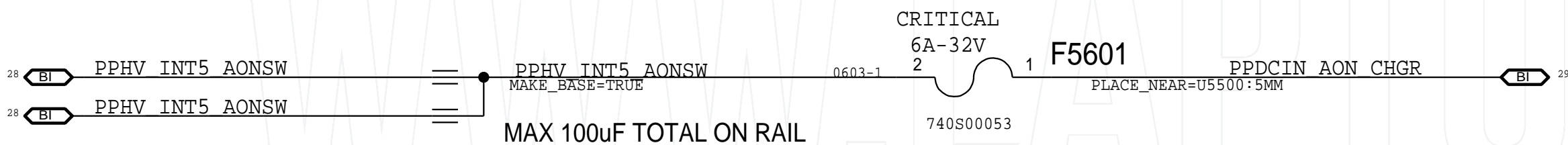


DEBUG PORT



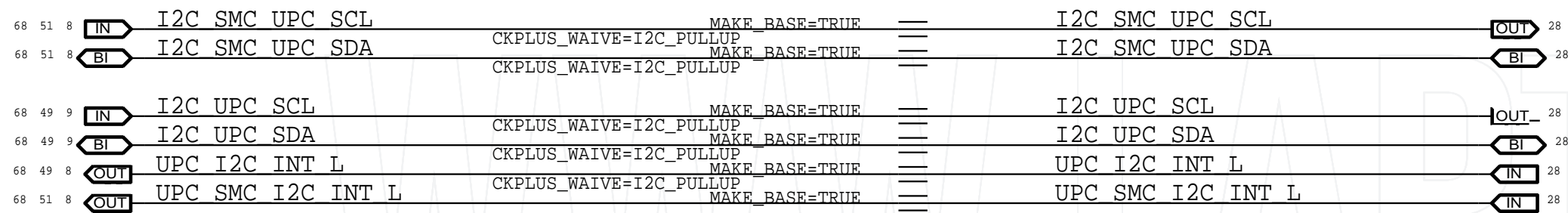
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B Power/Fuse for UPC5



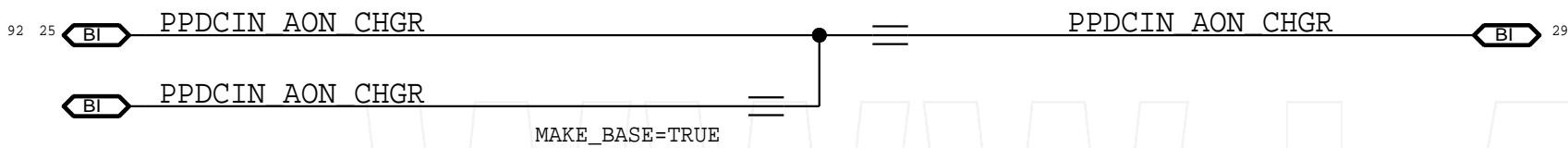
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C I2C Aliases



B

D Charger Aliases



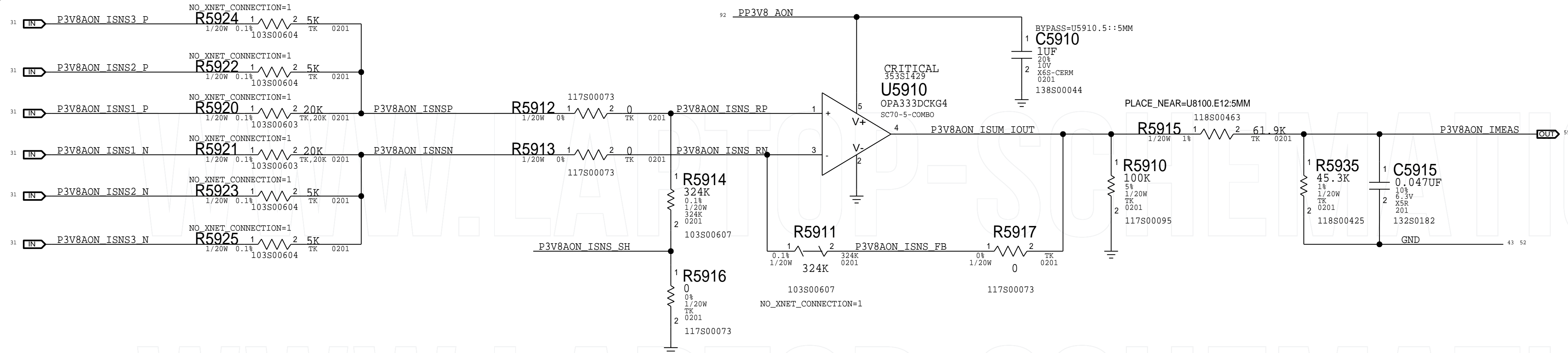
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	PAGE	56 OF 801
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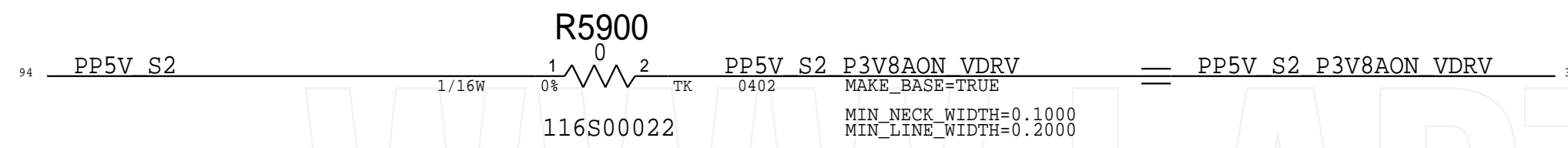
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Ⓐ PP3V8_AON Current Sense



Ⓑ PP5V_S2 to PP3V8_AON VDRV Connection

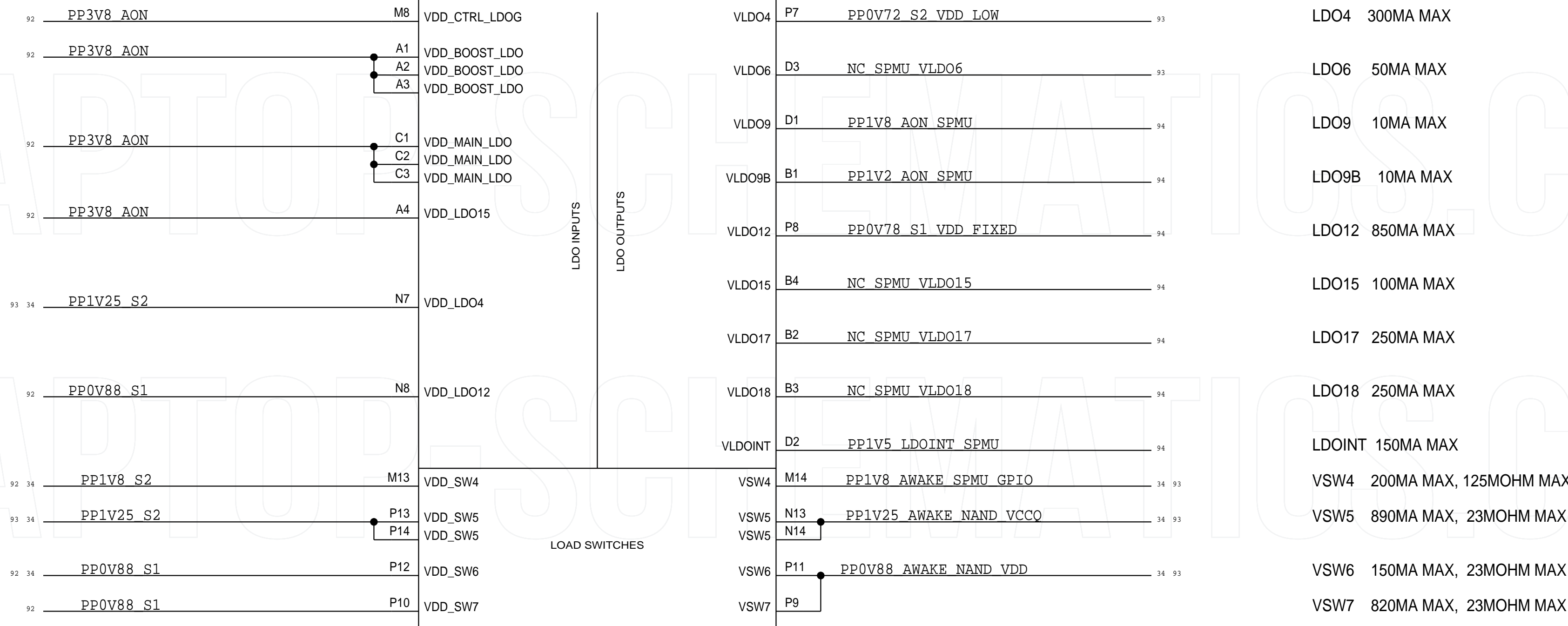




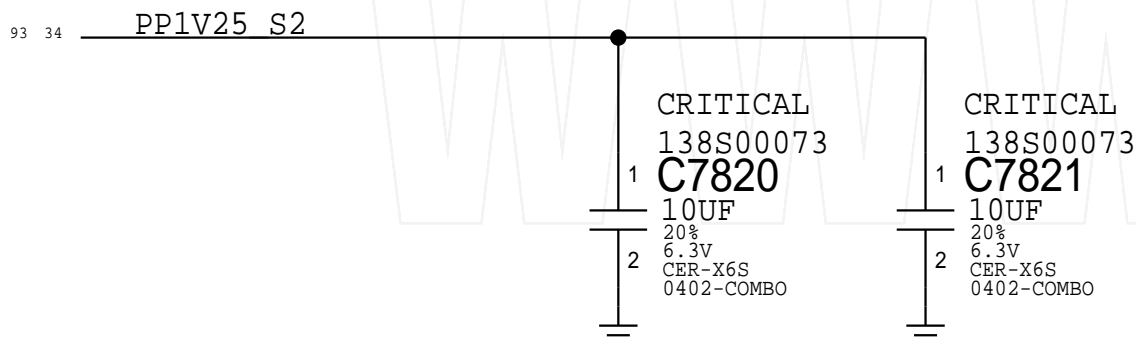
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 Apple Inc.	DRAWING NUMBER		SIZE
	051-07020		D
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		PAGE	
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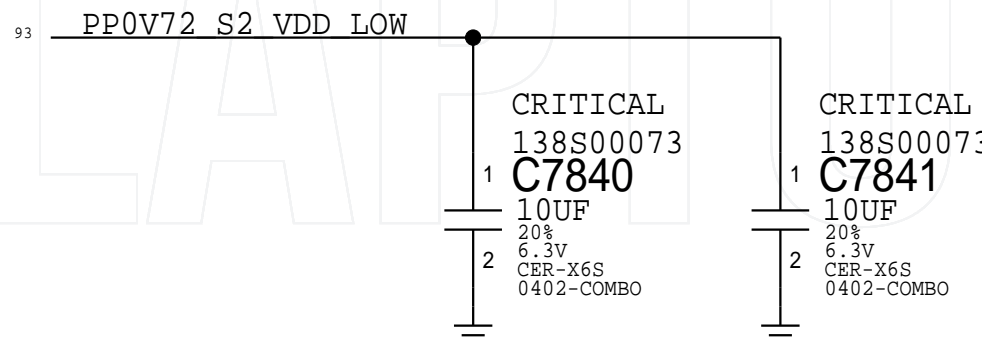
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998-23585
U7700
VALE
CSP
SYM 2 OF 4



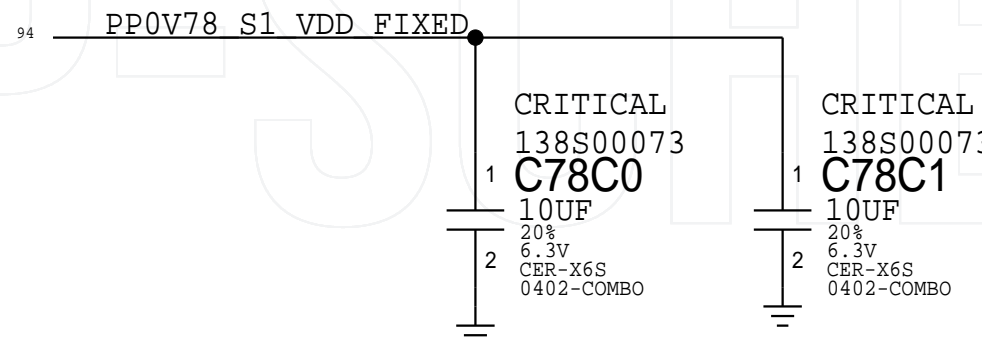
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DECOUPLNIG SHARED WITH J10 (VDDIO_1V2)



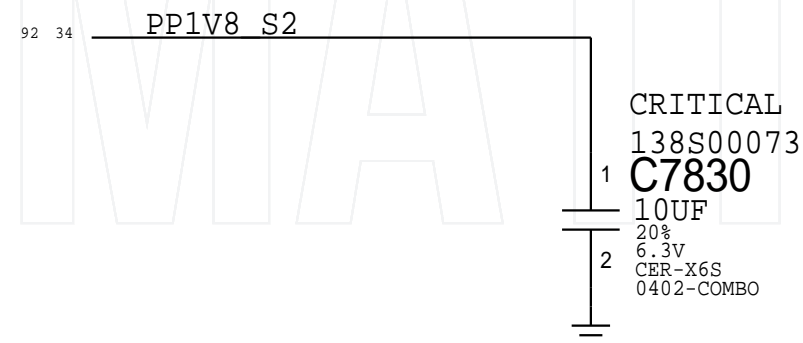
VLDO4



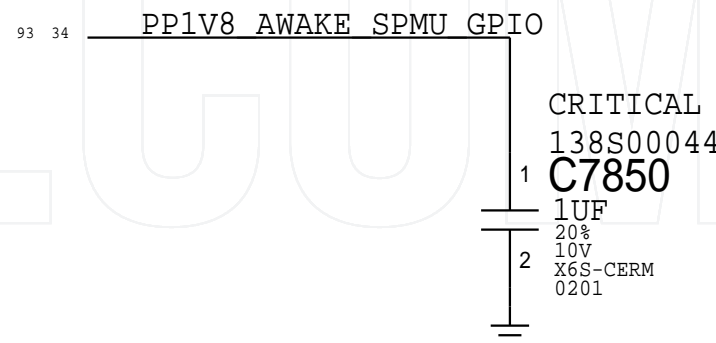
VLDO12



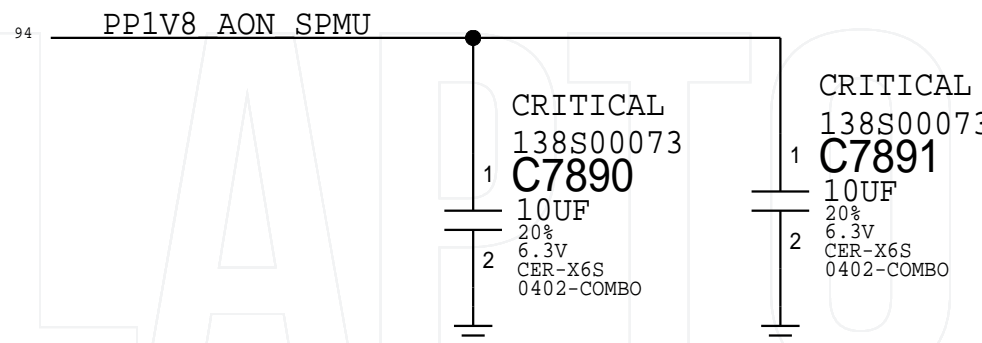
VDD_SW4
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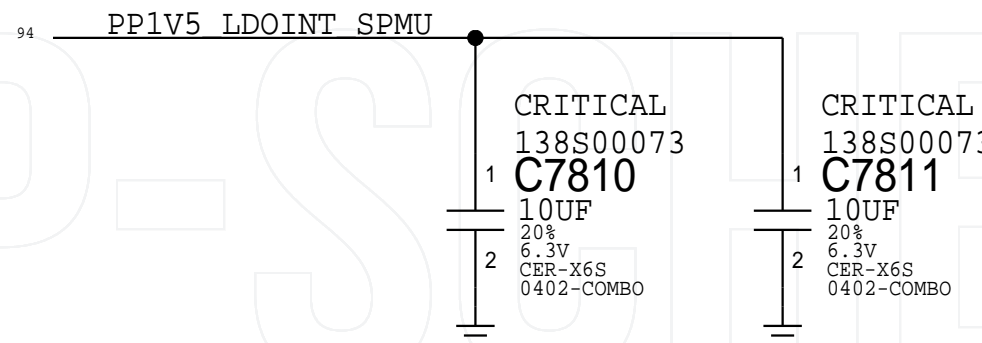
VSW4



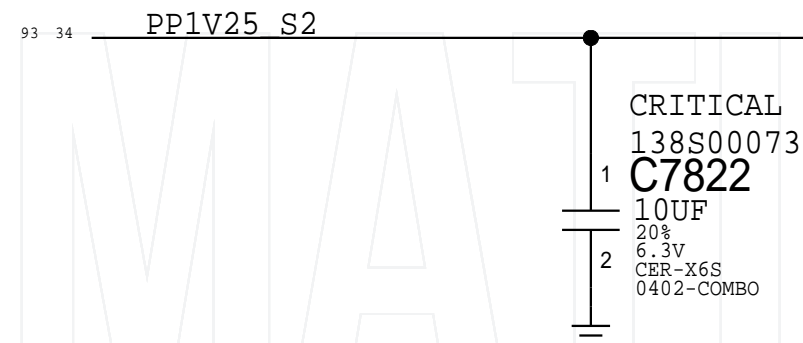
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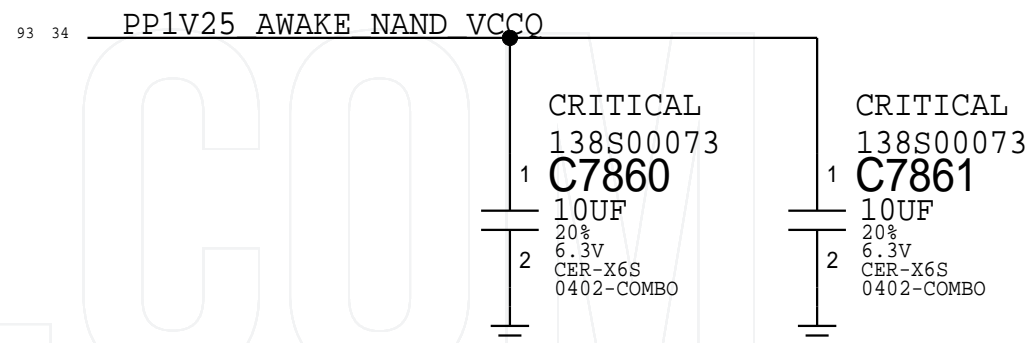
VLDOINT



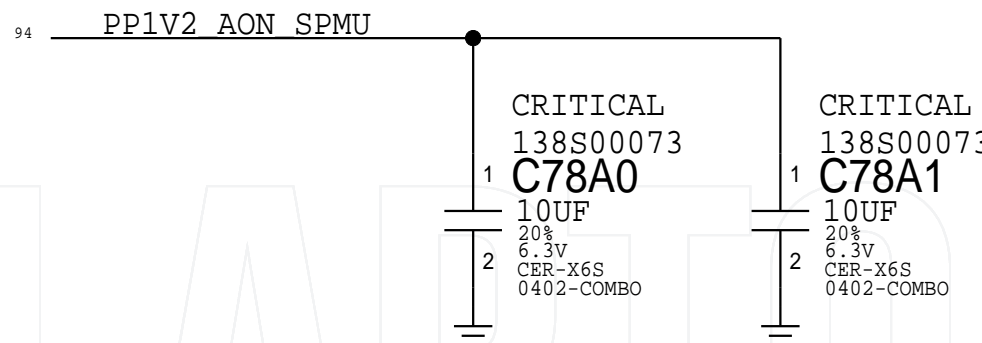
VDD_SW5
DECOUPLNIG SHARED WITH J10 (VDDIO_1V2)



VSW5



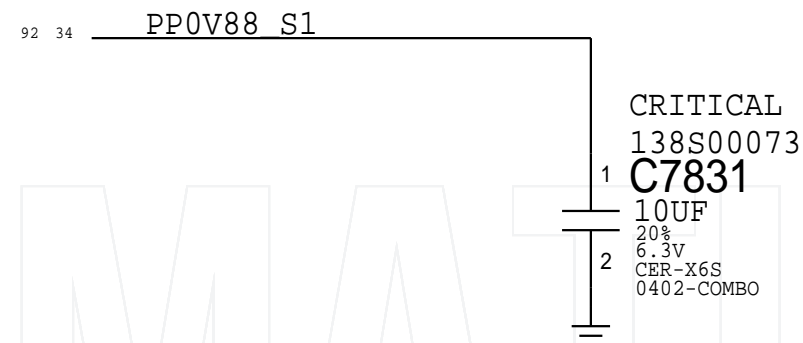
VLDO9B



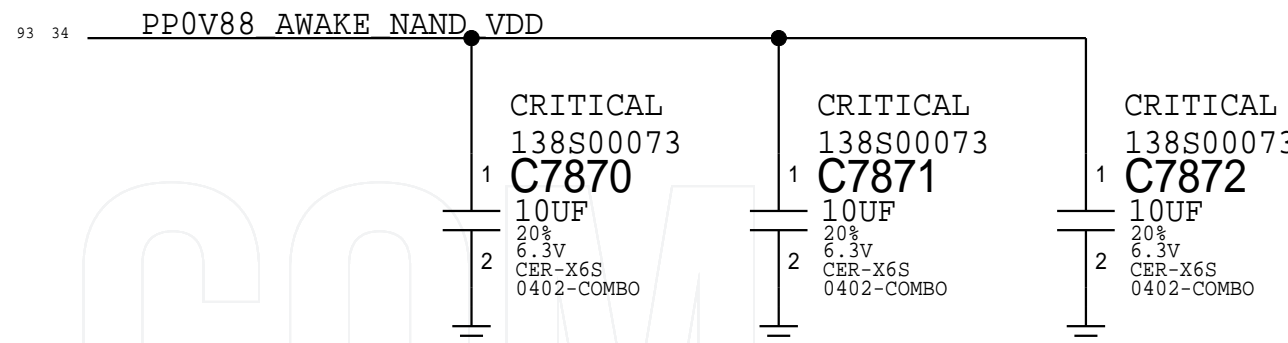
UN-UNUSED LDOS

LDO 6, 15, 17, 18

VDD_SW6/7
DECOUPLNIG SHARED VDD_LDO12



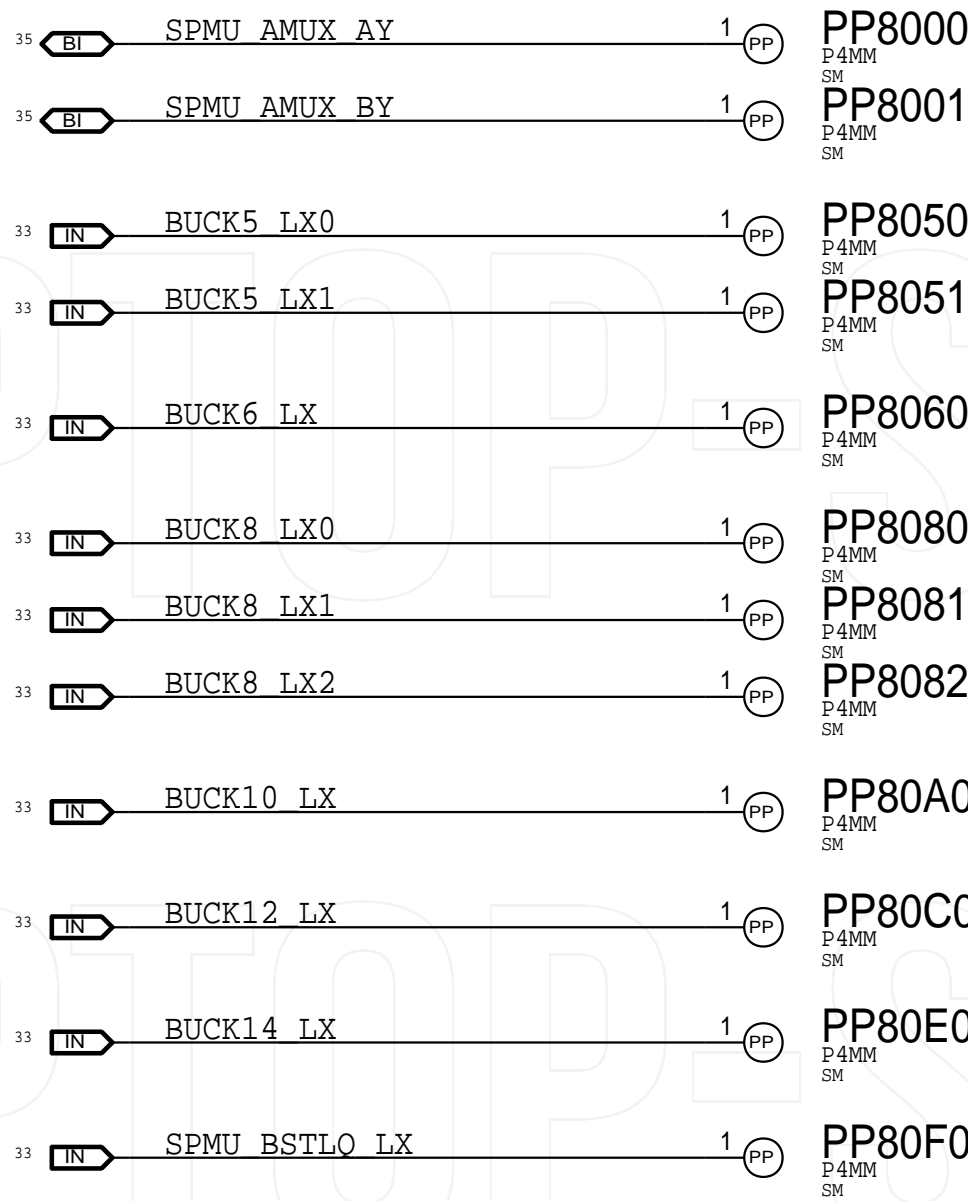
VSW6/7



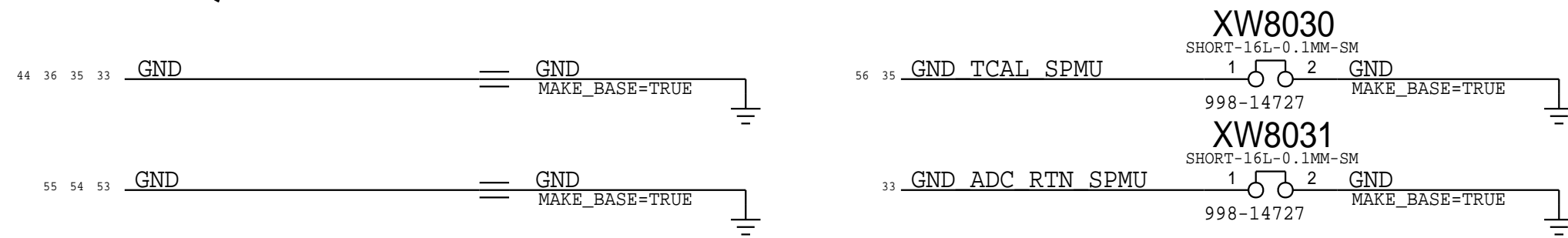
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	REVISION	6.0.0
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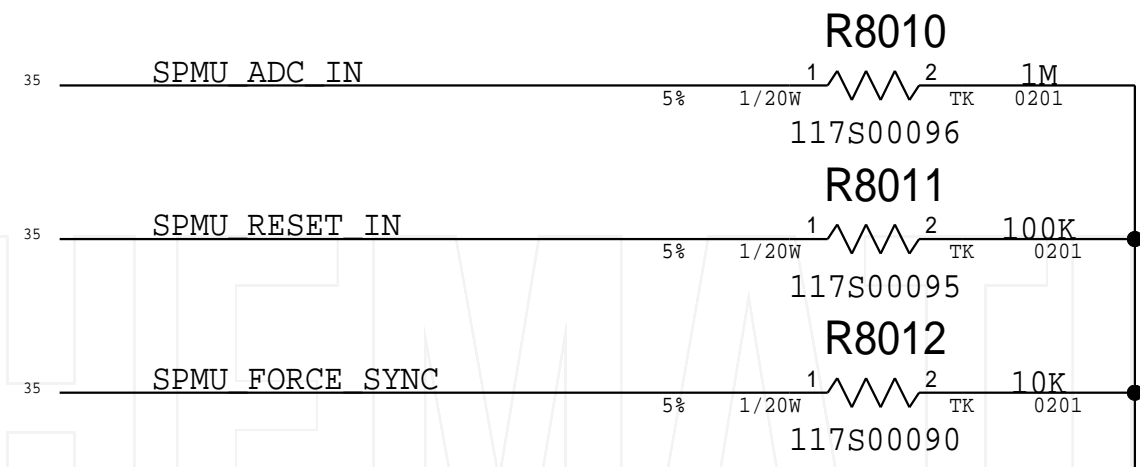
B Probe Points



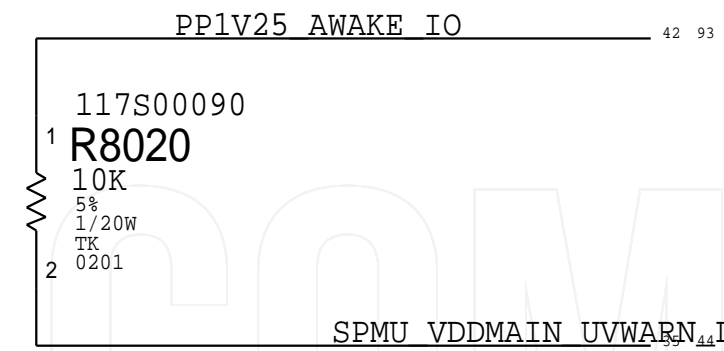
C SPMU Quiet GND Connections



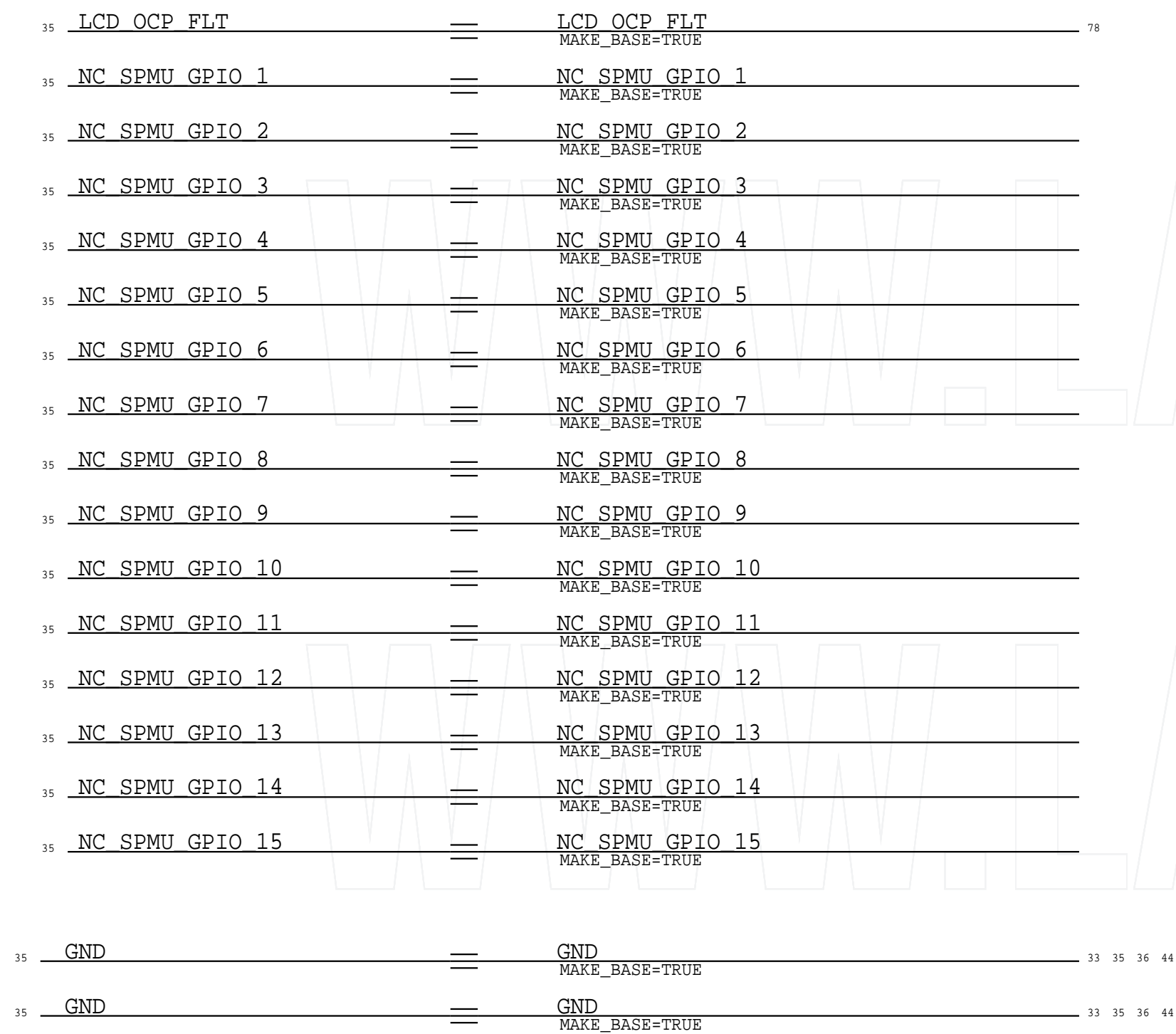
D SPMU Input Protection



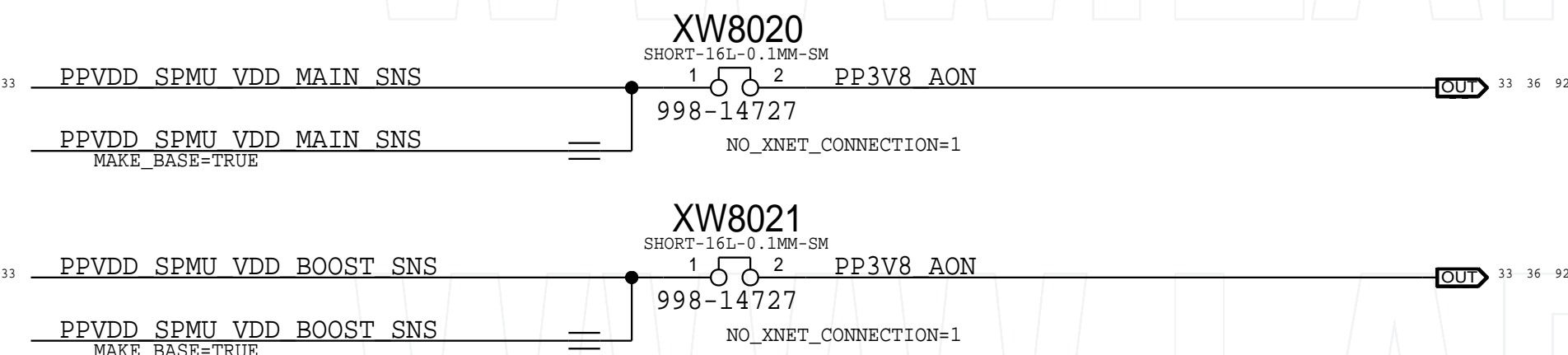
E SPMU/SOC Throttle Pull-Up



A SPMU GPIO



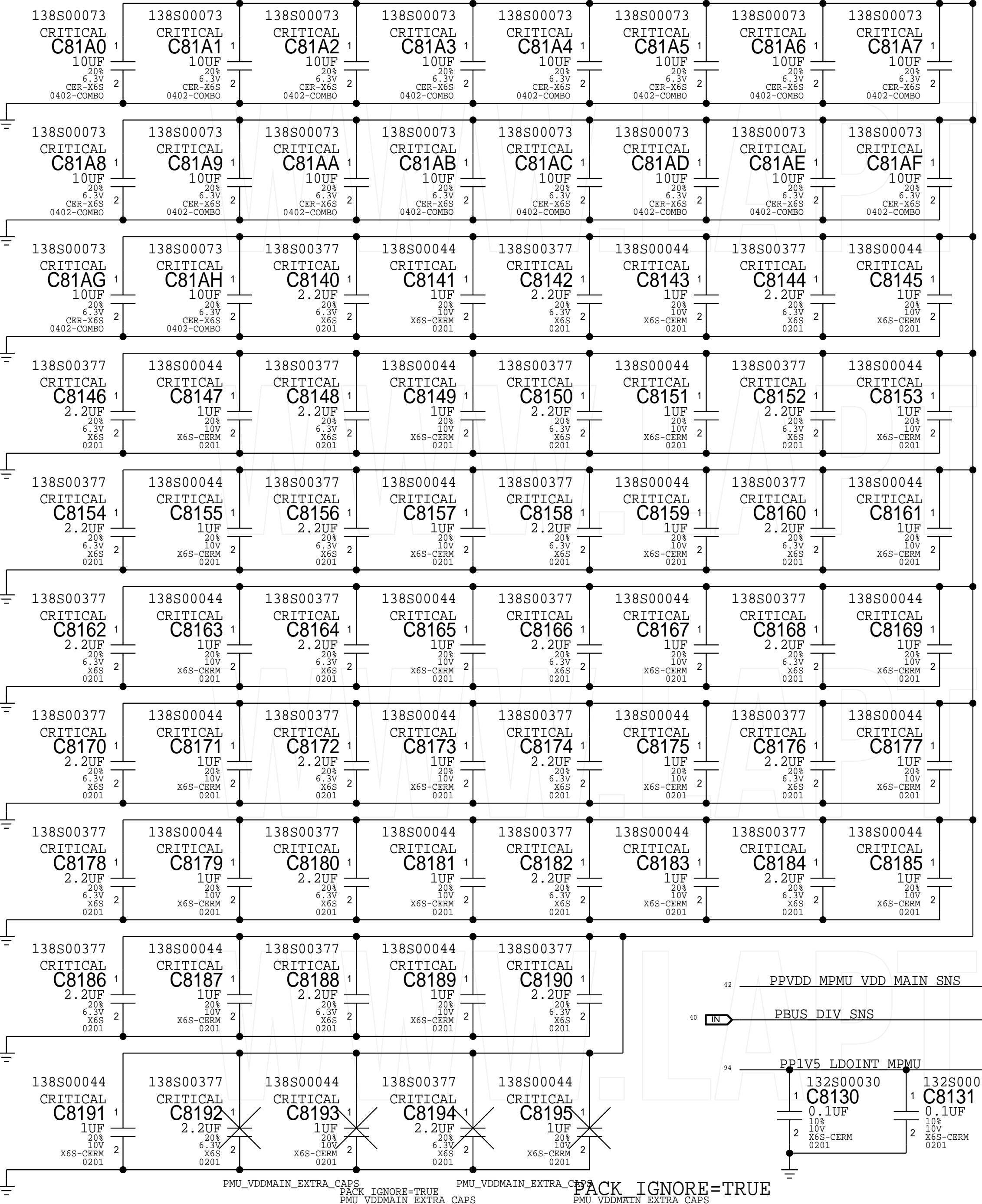
F SPMU Sense Connections



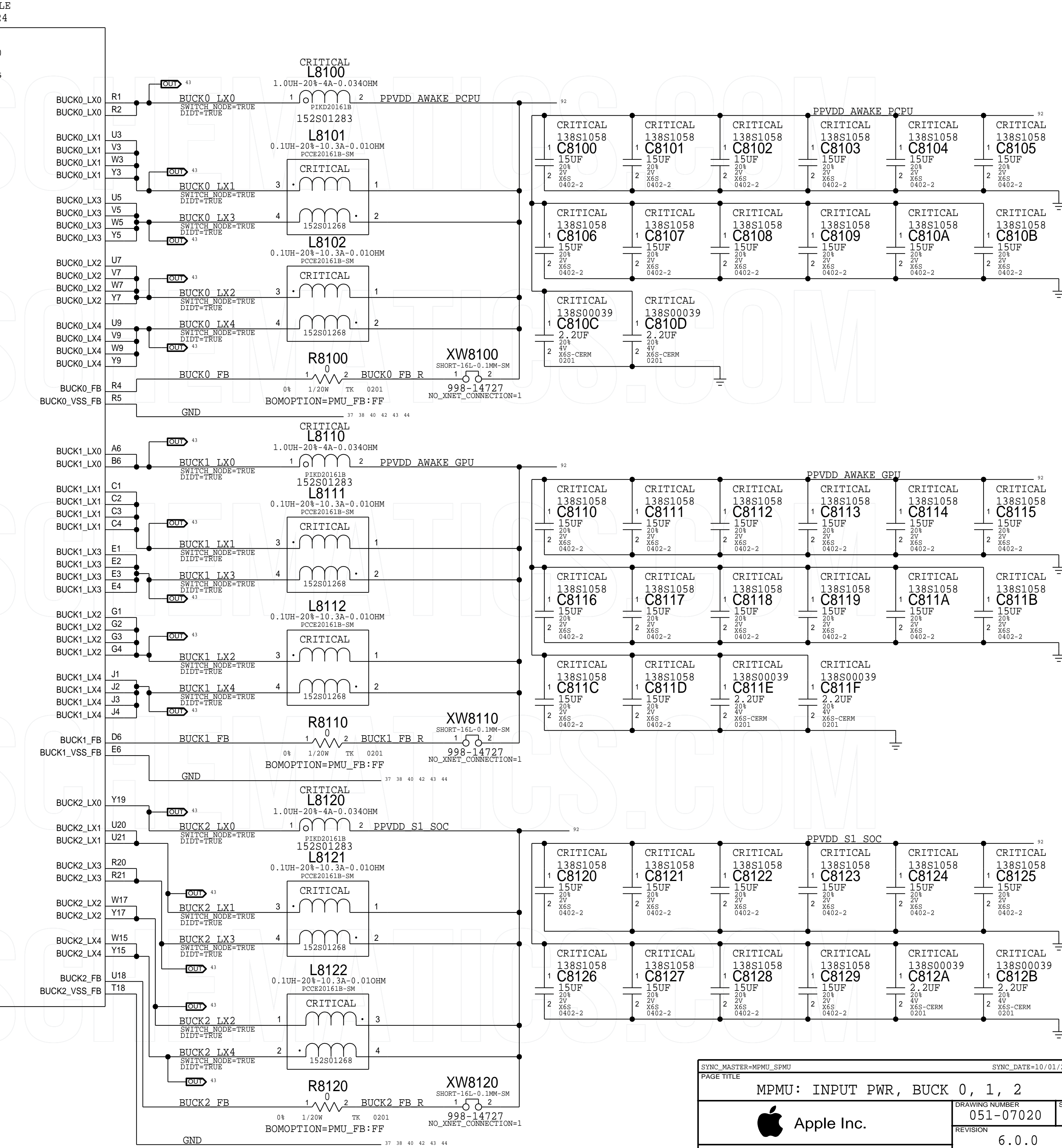
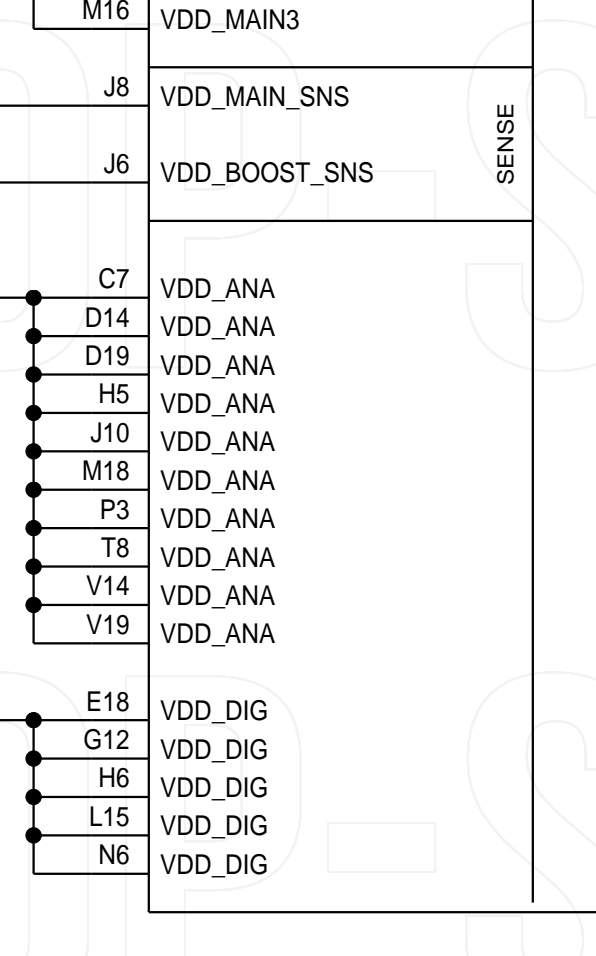
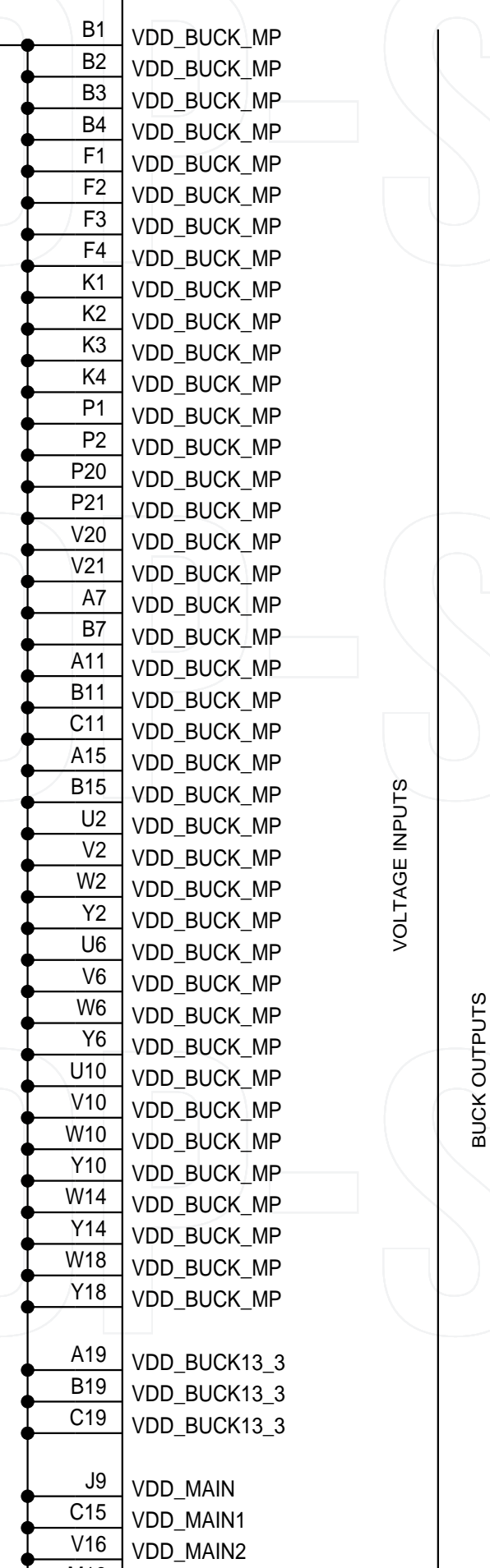
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Apple Inc.		REVISION		6.0.0	
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PP3V8 AON



OMIT_TABLE
998-23524
SYM 1 OF 5

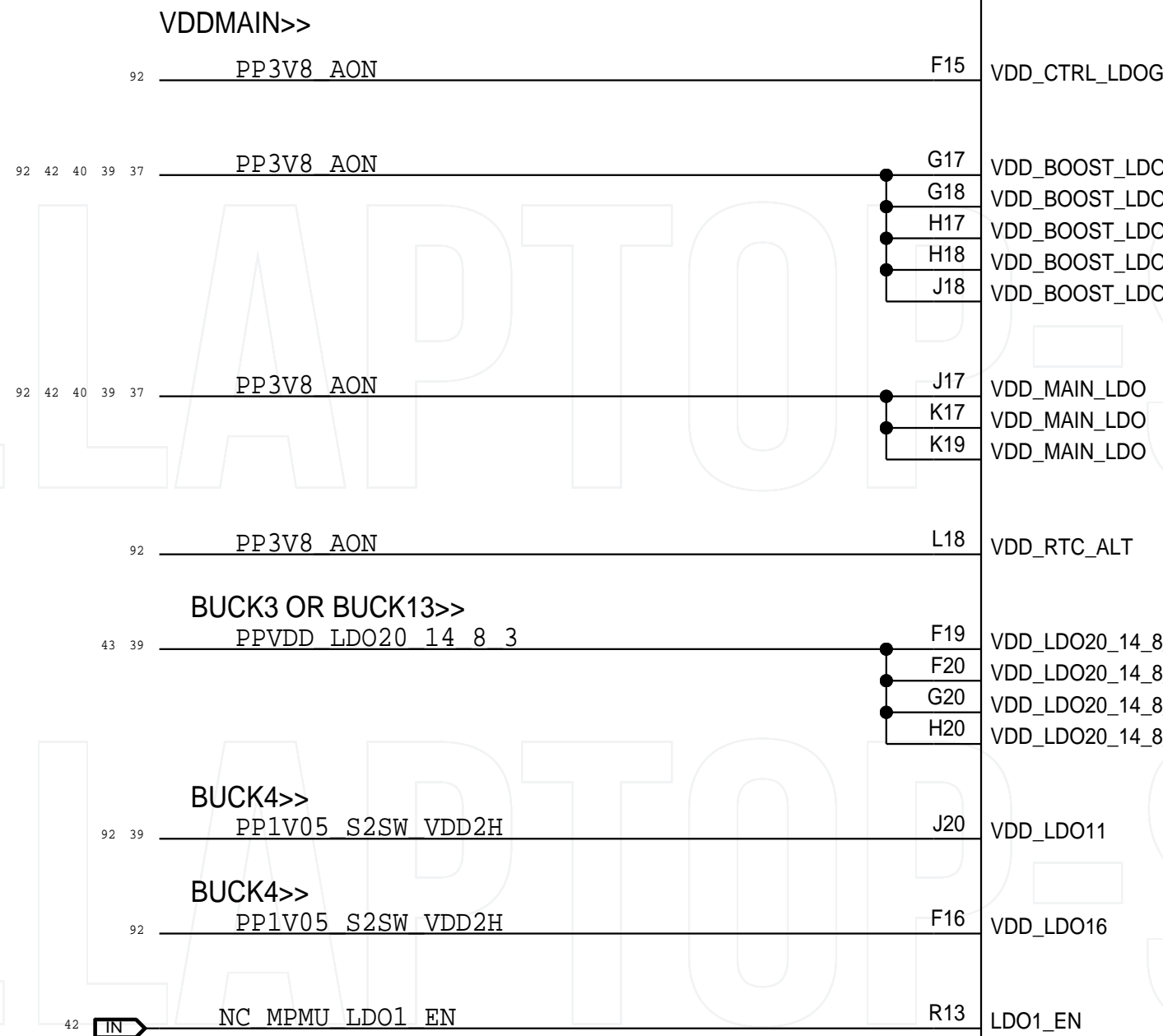


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DRAWING NUMBER		051-07020	SIZE D
REVISION		6.0.0	
BRANCH		evt-1	
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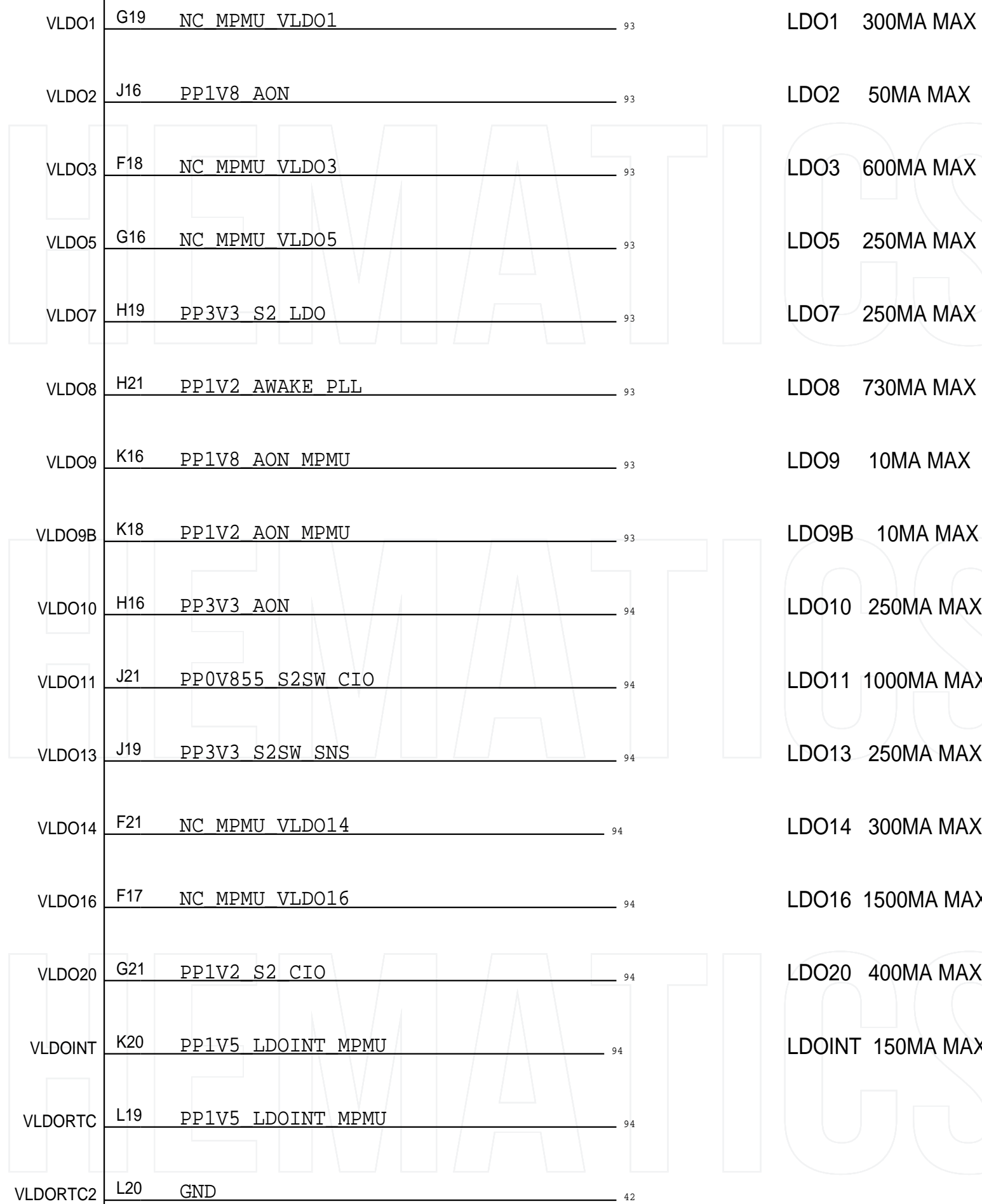
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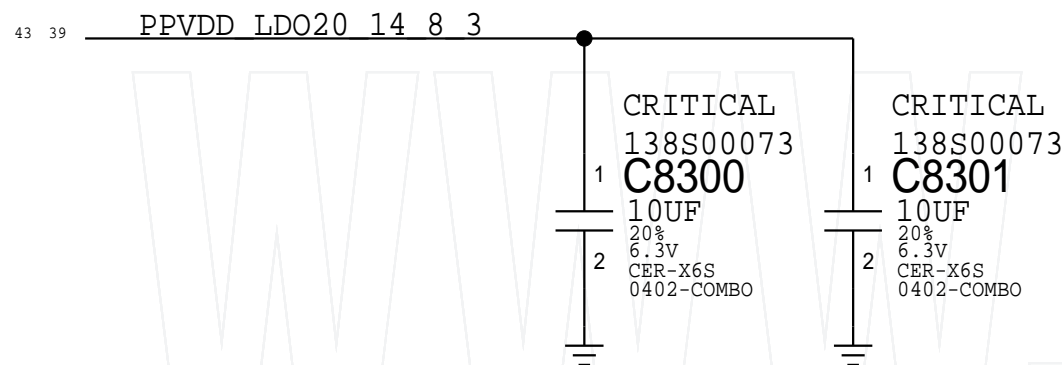
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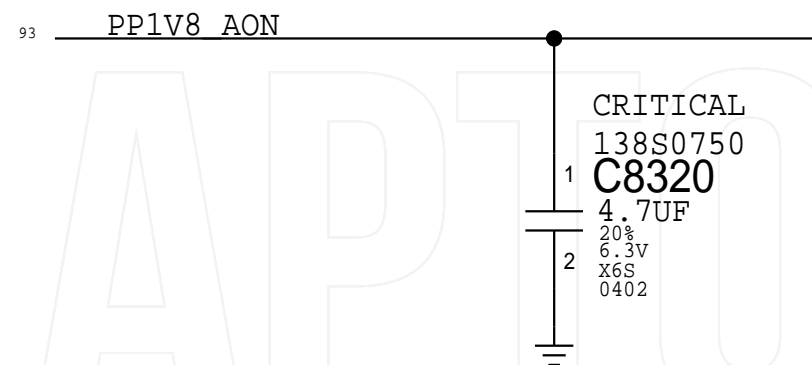
LDO INPUTS
LDO OUTPUTS



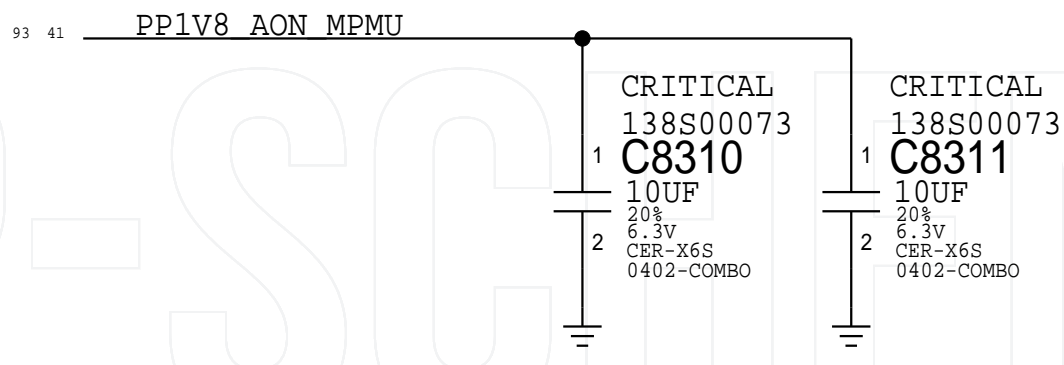
VDD LDO 3/8/14/20



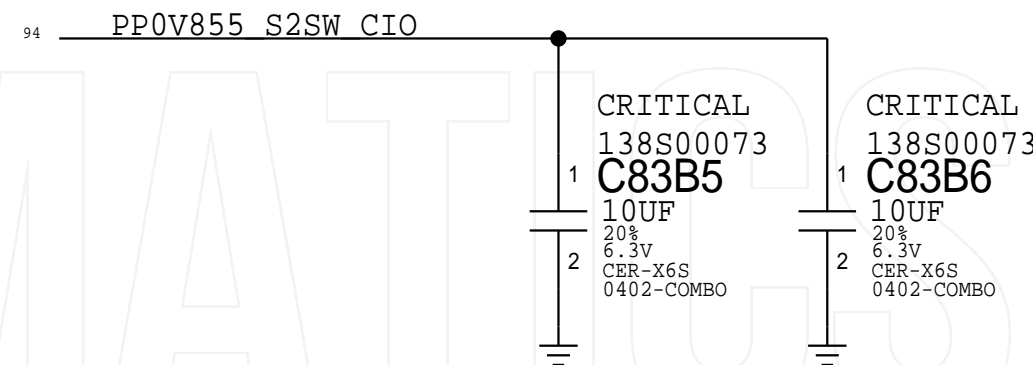
LDO 2 DECOUPLING



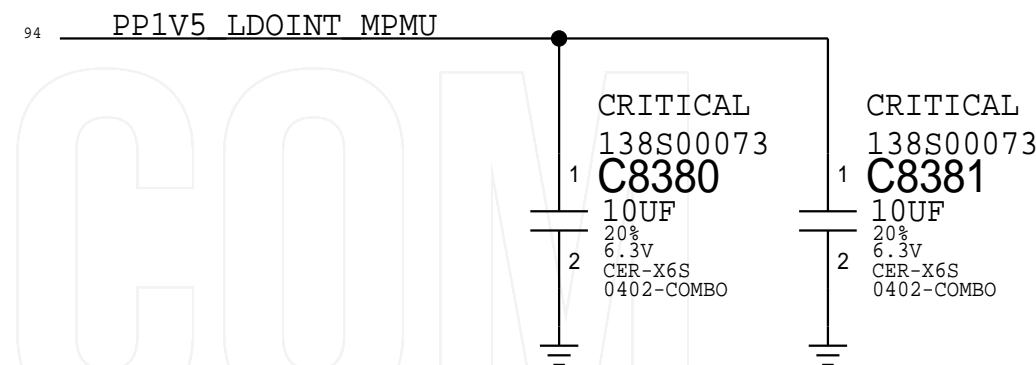
LDO 9 DECOUPLING



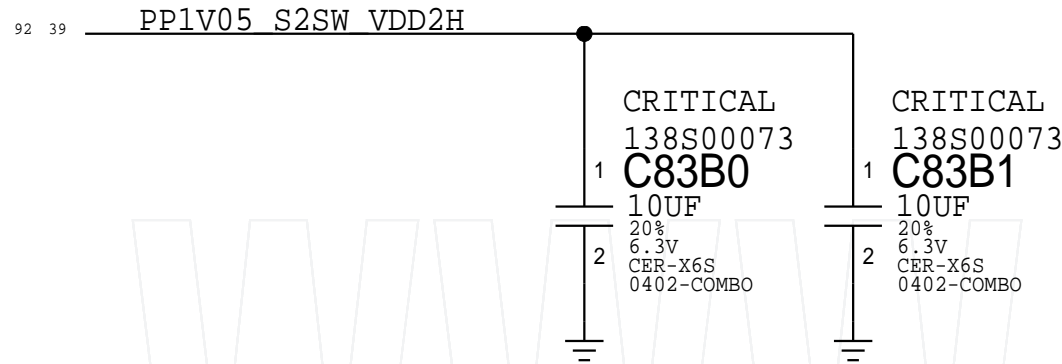
LDO 11 DECOUPLING



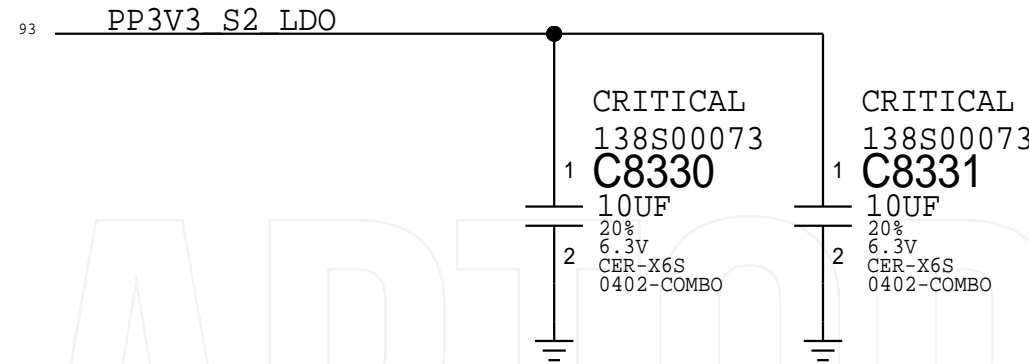
LDO INT DECOUPLING



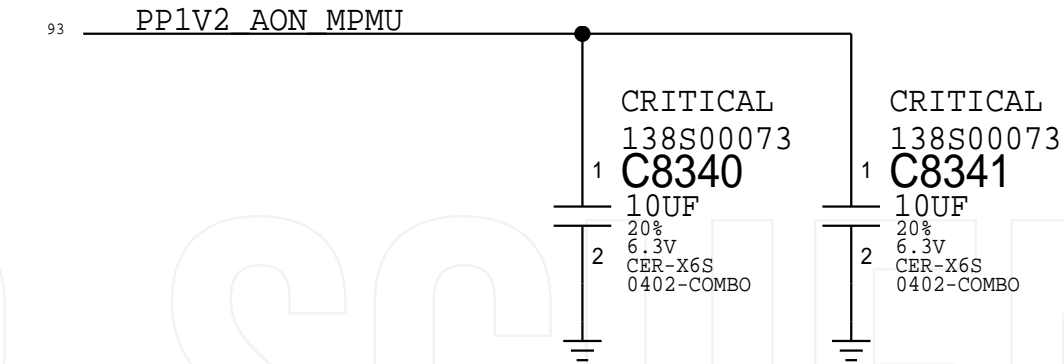
VDD LDO 11



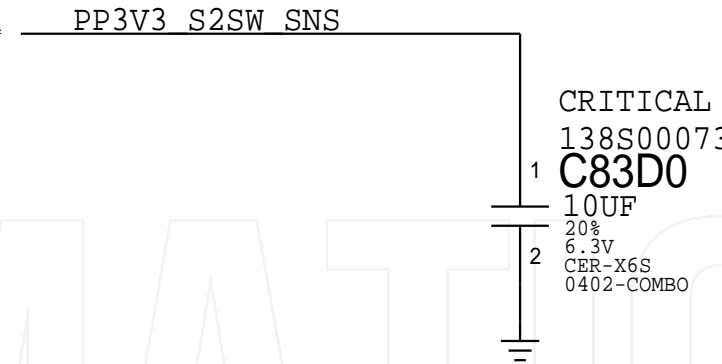
LDO 7 DECOUPLING



LDO 9B DECOUPLING



LDO 13 DECOUPLING



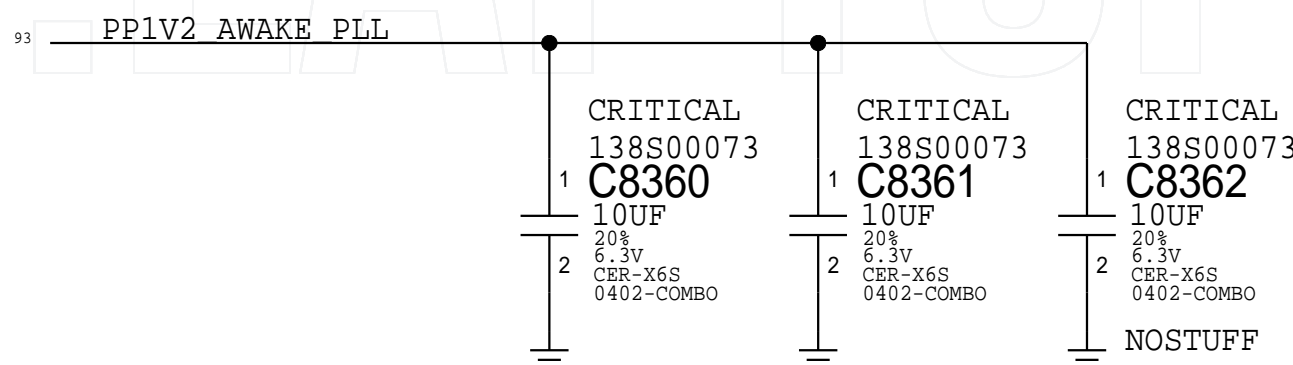
UN-UNUSED LDOS

LDO 1, 3, 5, 14, 16

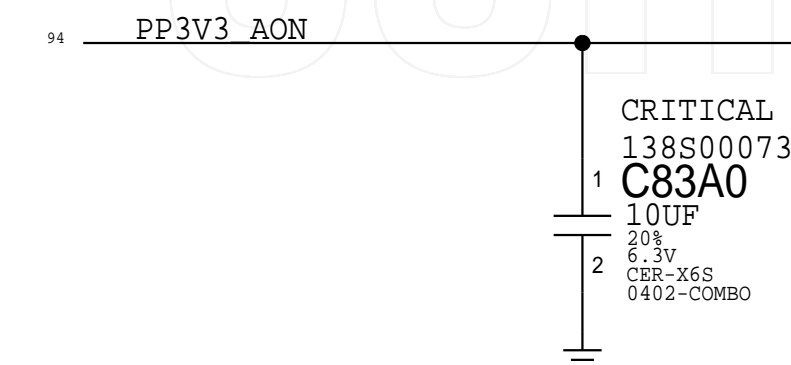
LDO RTC

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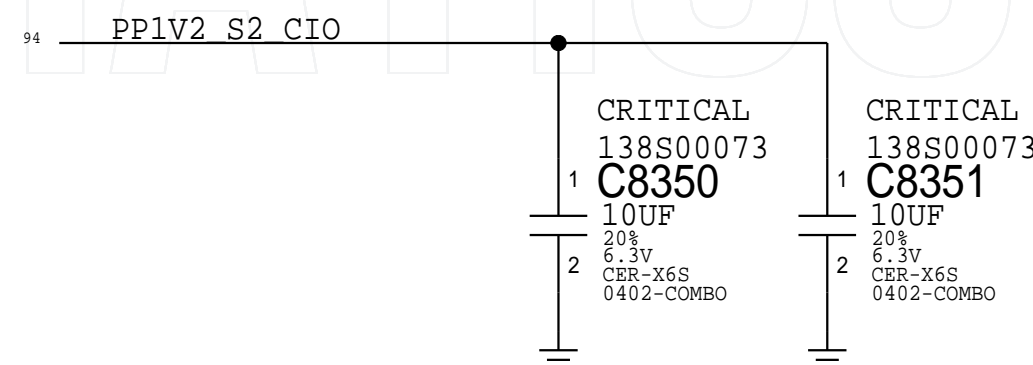
LDO 8 DECOUPLING




LDO 10 DECOUPLING



LDO 20 DECOUPLING

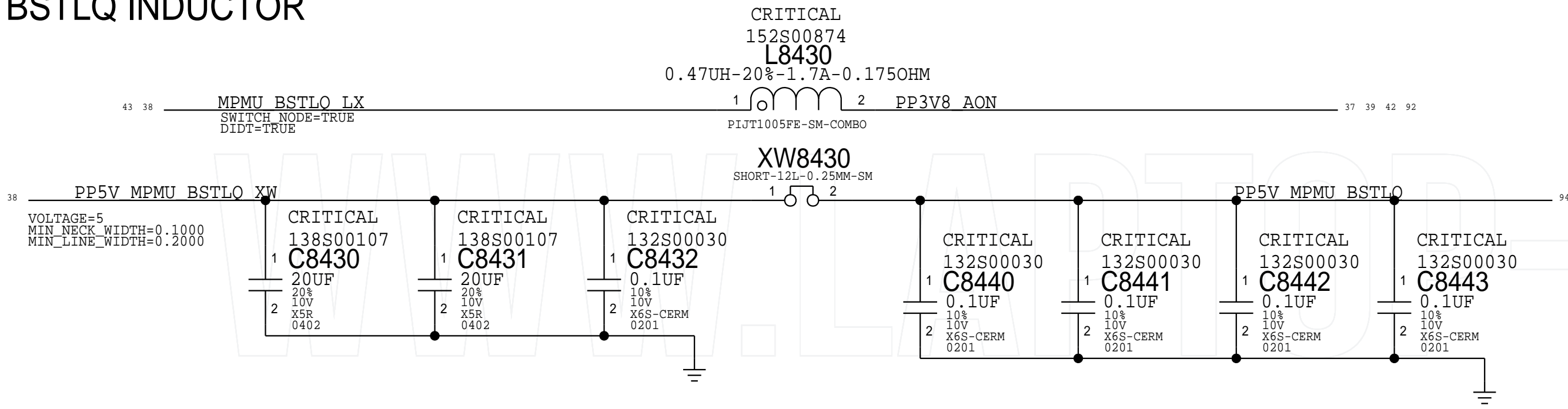


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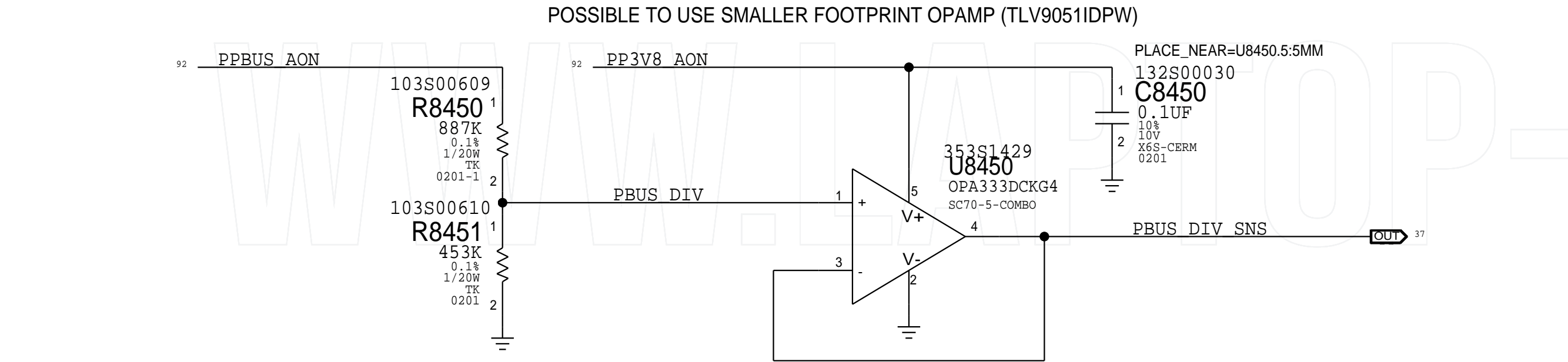
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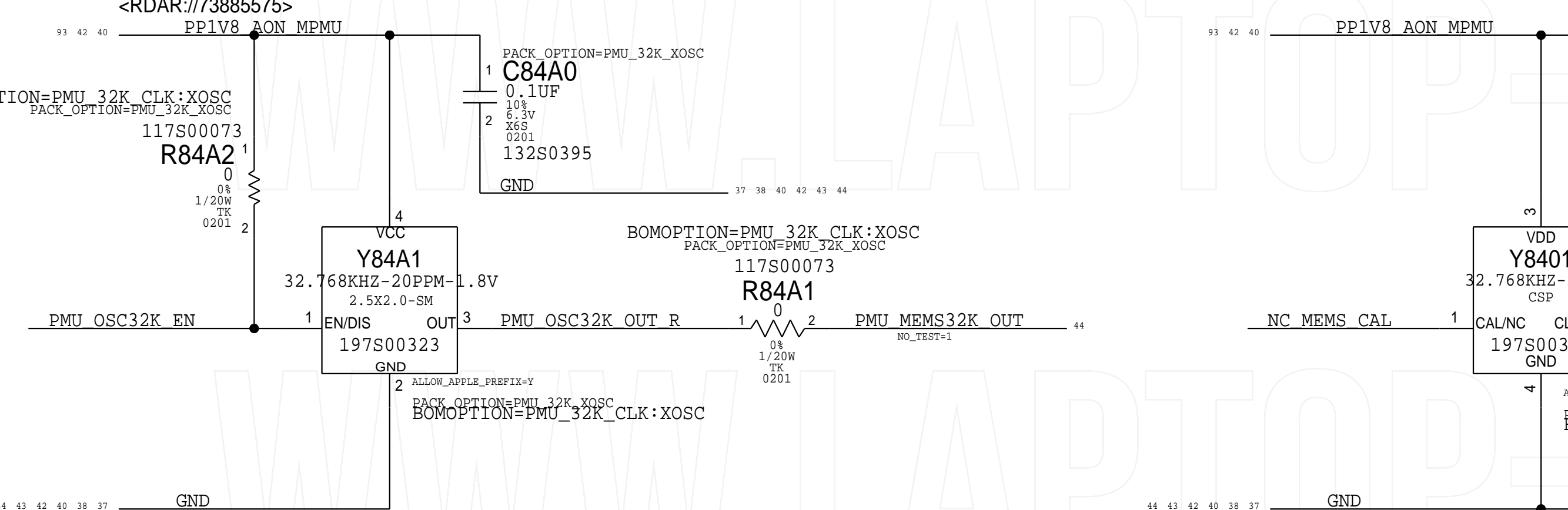
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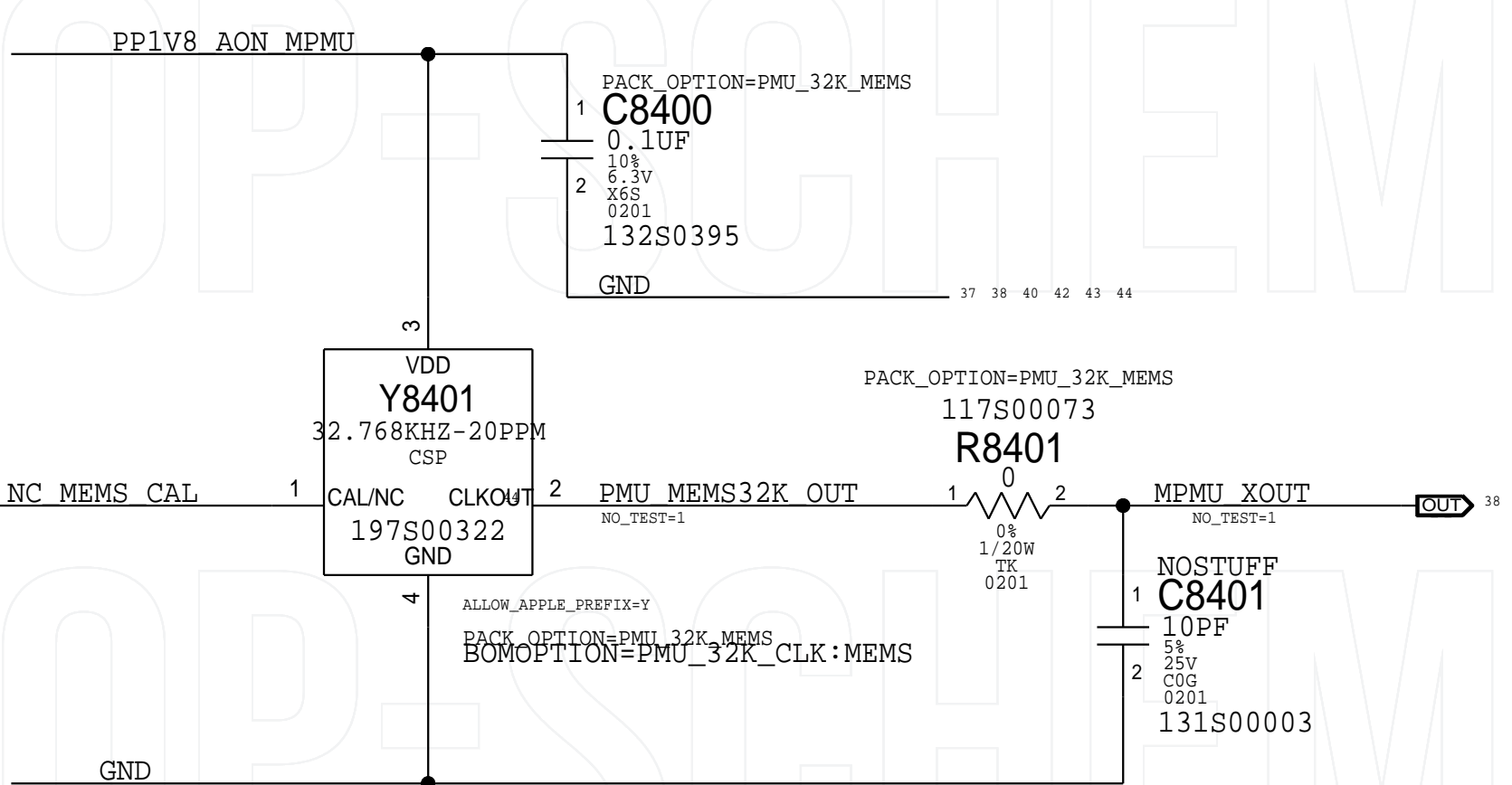
PBUS SENSE



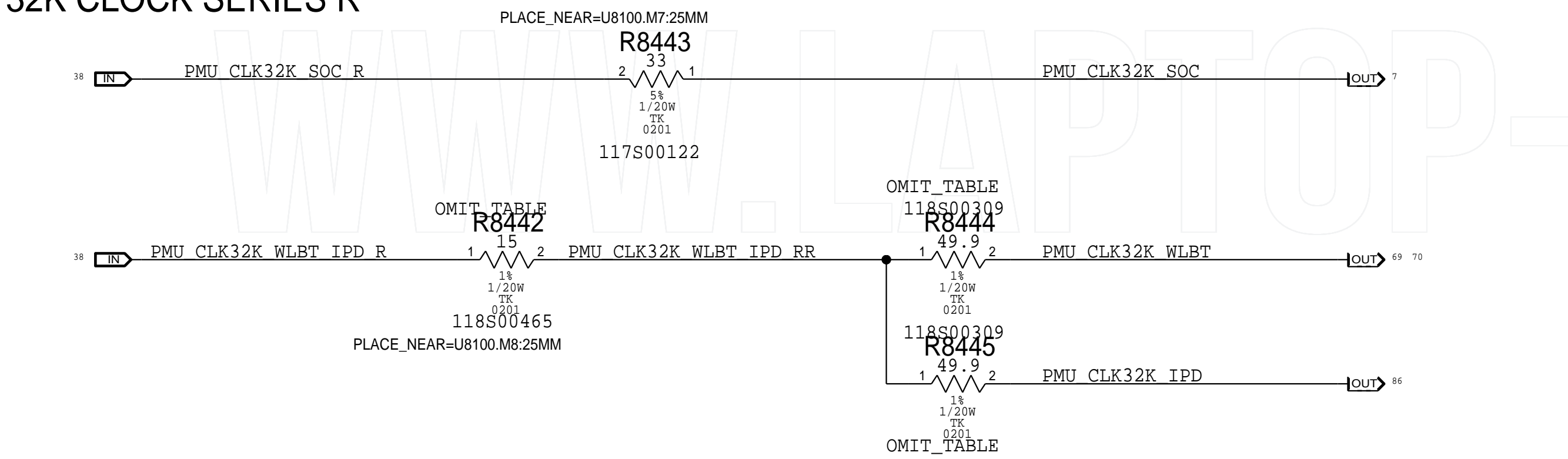
32K CLOCK XO (PACK_OPTION PMU_32K_OSC)



32K CLOCK MEMS (PACK_OPTION: PMU_32K_MEMS)



32K CLOCK SERIES R



PLACEMENT NOTES

CONNECT VSS_REF THROUGH ALL GND LAYERS
PLACE XW AT VSS_REF PIN, ROUTE RTN SIGNAL BACK TO PASSIVES

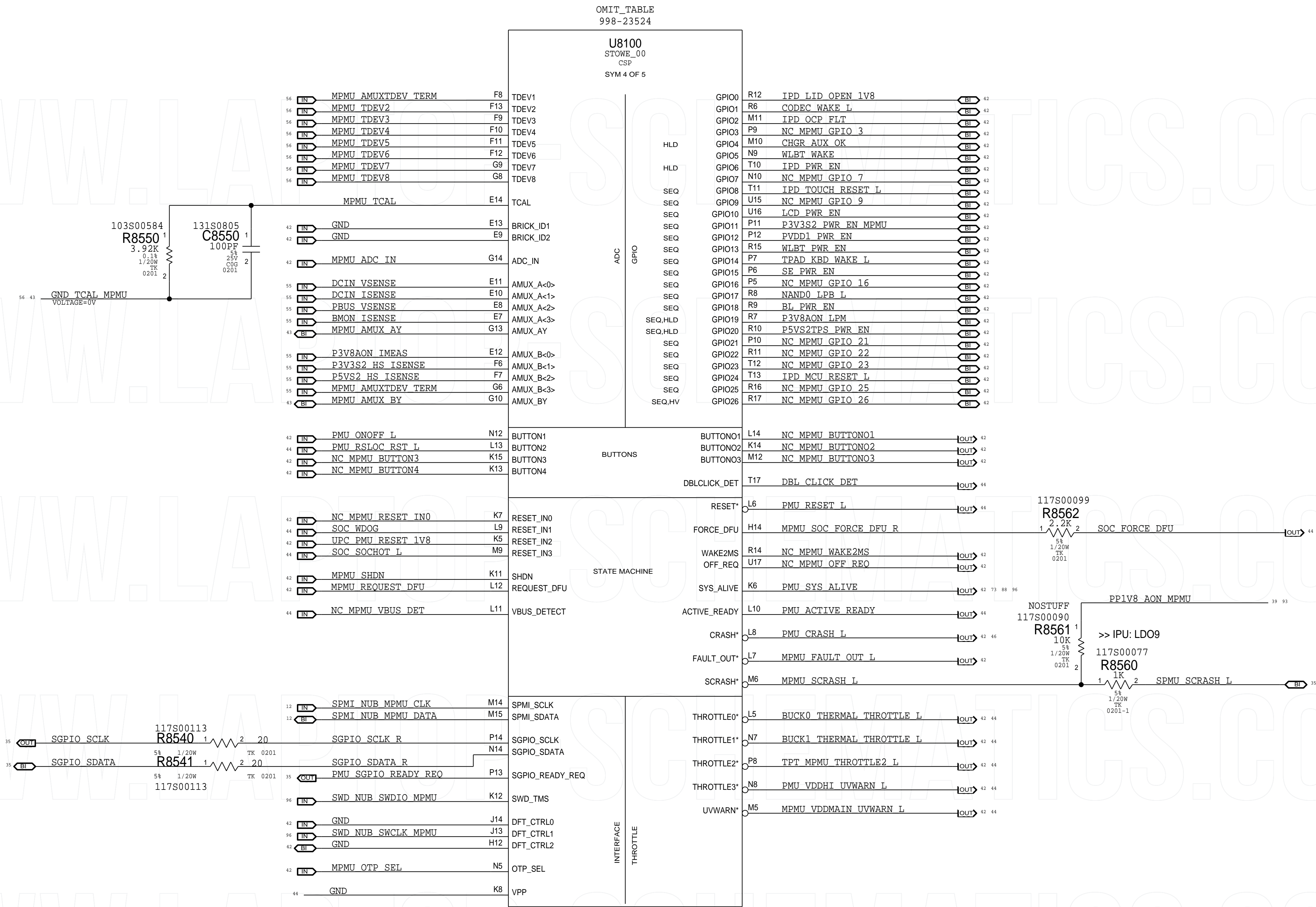
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118S00465	1	RES,TK,15 OHM,1%,1/20W,0201	R8442		PMU_OUT32K:TEE
117S00122	1	RES,TK,33 OHM,5%,1/20W,0201	R8442		PMU_OUT32K:WLBT
118S00309	2	RES,TK,49.9 OHM,1%,1/20W,0201	R8444,R8445		PMU_OUT32K:TEE
117S00073	1	RES,TK,0 OHM,1A MAX,1/20W,0201	R8444		PMU_OUT32K:WLBT


BOM_COST_GROUP=SOC POWER

PAGE_TITLE=MPMU: MISC CKT, VSS

PAGE TITLE		
Apple Inc.		
DRAWING NUMBER	051-07020	SIZE
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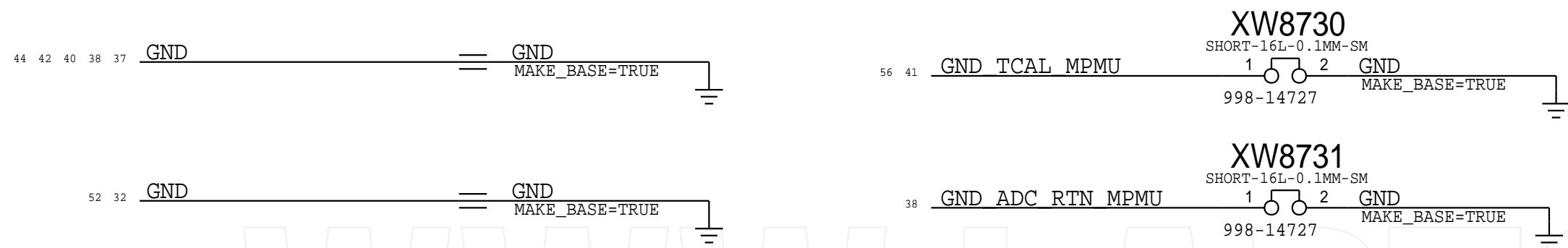
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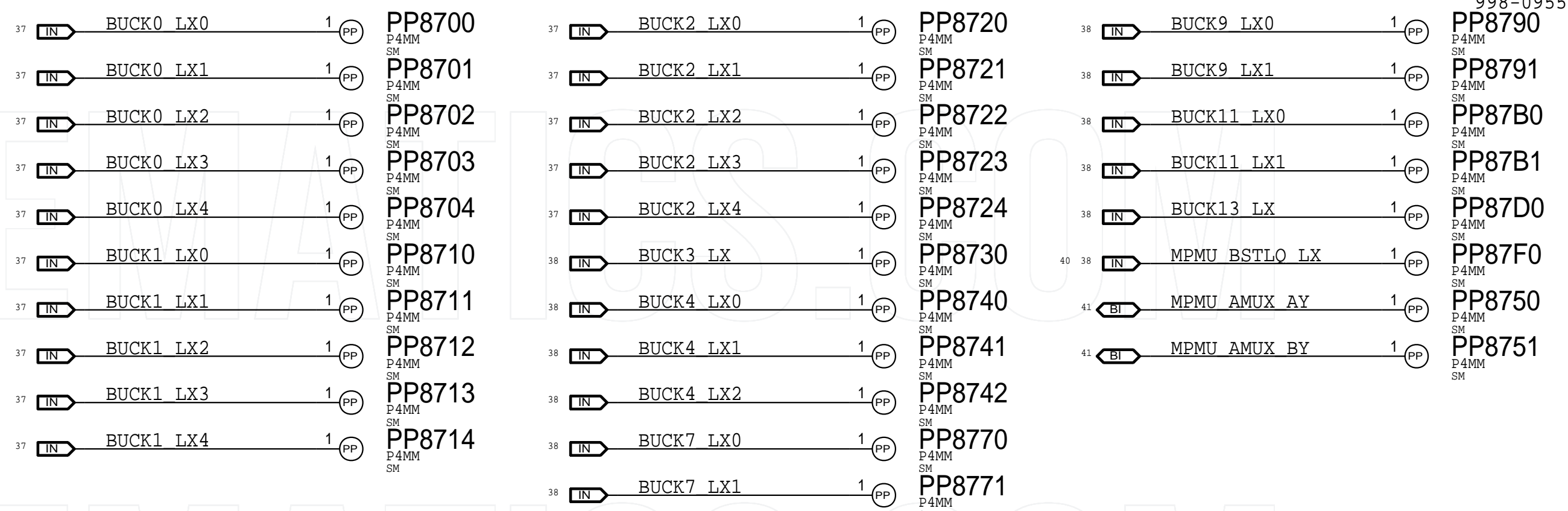
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		SHEET	41 OF 113

BOM_COST_GROUP=SOC POWER

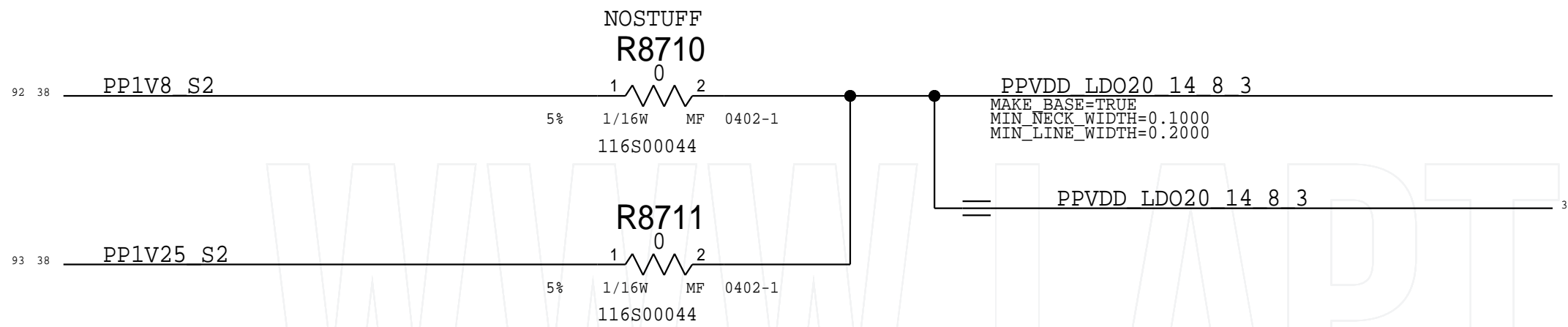
A MPMU Quiet GND Connections



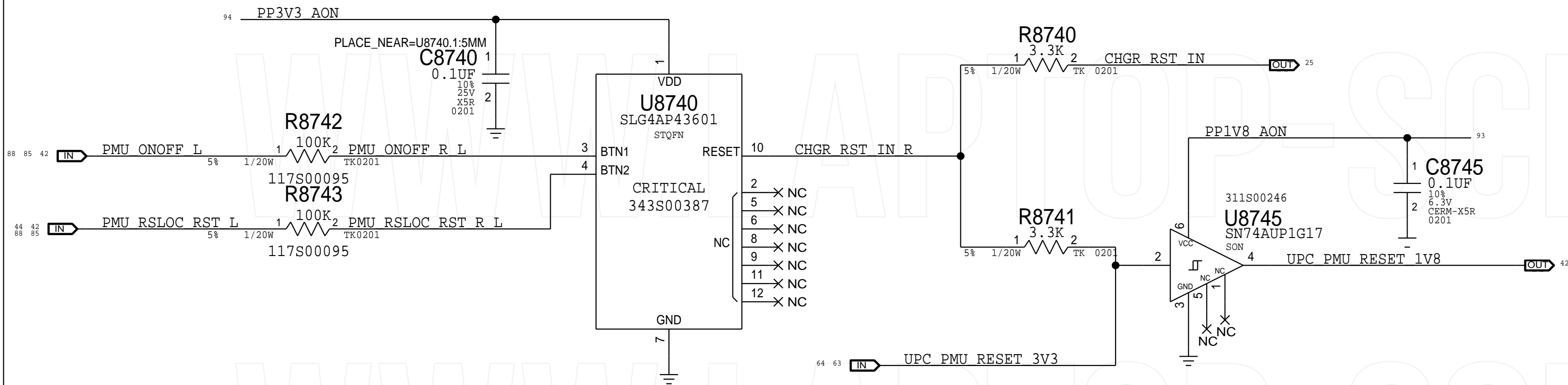
B MPMU Probe Points



C MPMU BUCK3/13 Option for LDO3/8/14/20 VDDIN



D MPMU Charger Reset Circuit



PAGE TITLE		
MPMU: SUPPORT		
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A

MPMU Misc Aliases

41	OUT	PMU_RSLOC_RST_L	==	PMU_RSLOC_RST_L MAKE_BASE=TRUE	42 43 85 88
38		NC_MPMU_XIN	==	NC_MPMU_XIN MAKE_BASE=TRUE	
41		SOC_WDOG	==	SOC_WDOG MAKE_BASE=TRUE	7
41		SOC_SOCHOT_L	==	SOC_SOCHOT_L MAKE_BASE=TRUE	9
41		PMU_RESET_L	==	PMU_RESET_L MAKE_BASE=TRUE	7 88
41		PMU_ACTIVE_READY	==	PMU_ACTIVE_READY MAKE_BASE=TRUE	7 61 88
41		DBL_CLICK_DET	==	DBL_CLICK_DET MAKE_BASE=TRUE	9
41		SOC_FORCE_DFU	==	SOC_FORCE_DFU MAKE_BASE=TRUE	7 42 62 88
42		BUCK0_THERMAL_THROTTLE_L	==	BUCK0_THERMAL_THROTTLE_L MAKE_BASE=TRUE	9
42		BUCK1_THERMAL_THROTTLE_L	==	BUCK1_THERMAL_THROTTLE_L MAKE_BASE=TRUE	9
42		TPT_MPMU_THROTTLE2_L	==	TPT_MPMU_THROTTLE2_L MAKE_BASE=TRUE	
42	41	PMU_VDDHI_UVWARN_L	==	PMU_VDDHI_UVWARN_L MAKE_BASE=TRUE	9
42	41	MPMU_VDDMAIN_UVWARN_L	==	MPMU_VDDMAIN_UVWARN_L MAKE_BASE=TRUE	9
41		NC_MPMU_VBUS_DET	==	NC_MPMU_VBUS_DET MAKE_BASE=TRUE	
41		GND	==	GND MAKE_BASE=TRUE	37 38 40 42 43

B


SPMU Misc Aliases

9		SPMU_VDDMAIN_UVWARN_L	==	SPMU_VDDMAIN_UVWARN_L MAKE_BASE=TRUE	44
36 35		SPMU_VDDMAIN_UVWARN_L	==	SPMU_VDDMAIN_UVWARN_L MAKE_BASE=TRUE	44
35		GND	==	GND MAKE_BASE=TRUE	33 35 36

C

32.768kHz Clock Aliases

40		PMU_MEMS32K_OUT	==	PMU_MEMS32K_OUT MAKE_BASE=TRUE	40
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BOM_COST_GROUP=SOC POWER

* OK2INTEGRATE *

5V_S2 Voltage Regulator

SET ONE OPTION FOR THE PBUS POLY CAPS

PACK_OPTION=5V_S2_PBUS-B12
PACK_OPTION=5V_S2_PBUS-D2
PACK_OPTION=5V_S2_PBUS-D12
PACK_OPTION=5V_S2_PBUS18V

SET ONE OPTION FOR THE OUTPUT CAPS

PACK_OPTION=5V_S2_VOUT-B2
PACK_OPTION=5V_S2_VOUT-B12

SET ONE OPTION FOR THE INDUCTOR

PACK_OPTION=5V_S2_IND-24
PACK_OPTION=5V_S2_IND-15

SET ONE OPTION FOR THE MLCC CAPS

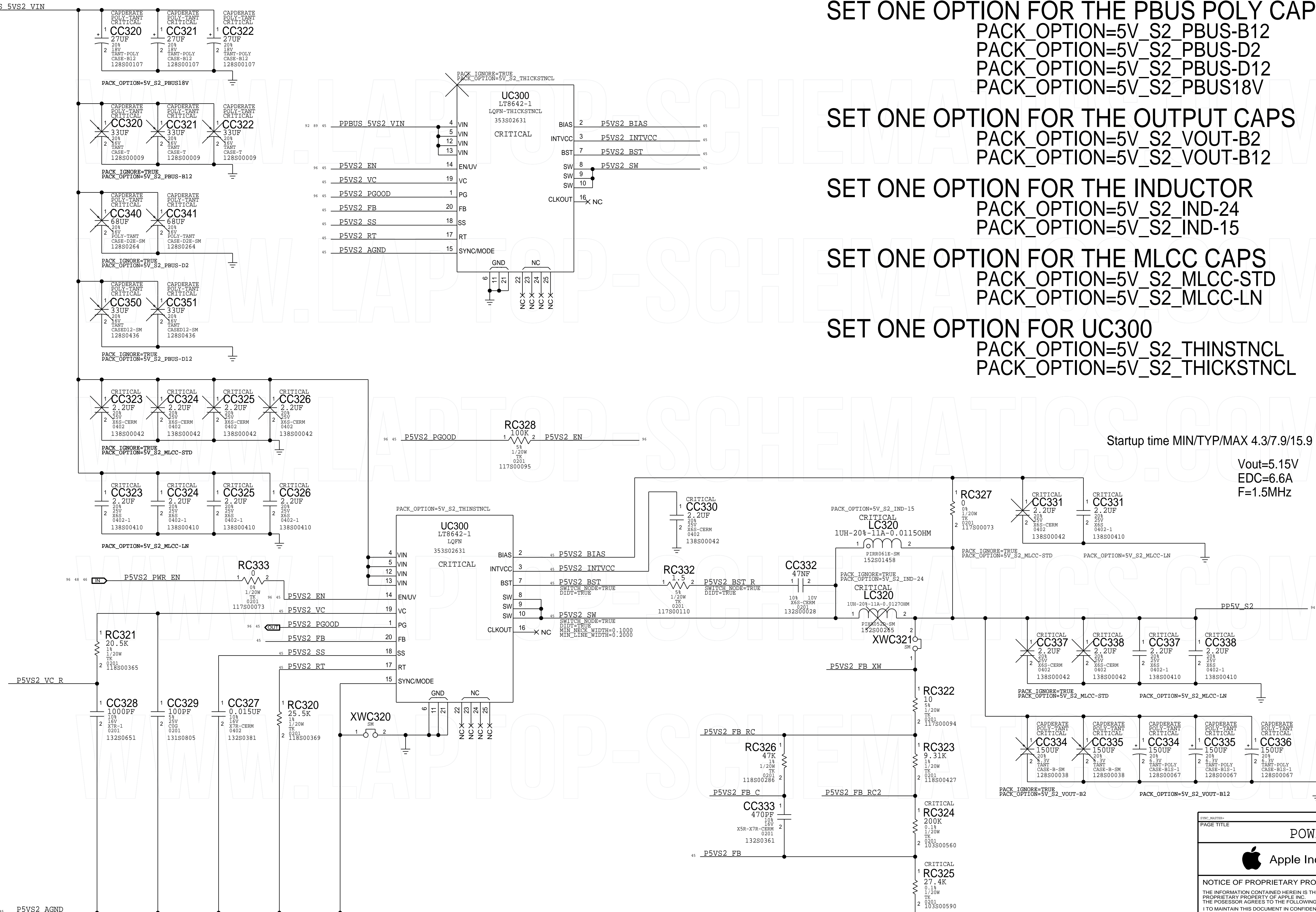
PACK_OPTION=5V_S2_MLCC-STD
PACK_OPTION=5V_S2_MLCC-LN

SET ONE OPTION FOR UC300

PACK_OPTION=5V_S2_THINSTNCL
PACK_OPTION=5V_S2_THICKSTNCL

Startup time MIN/TYP/MAX 4.3/7.9/15.9 ms

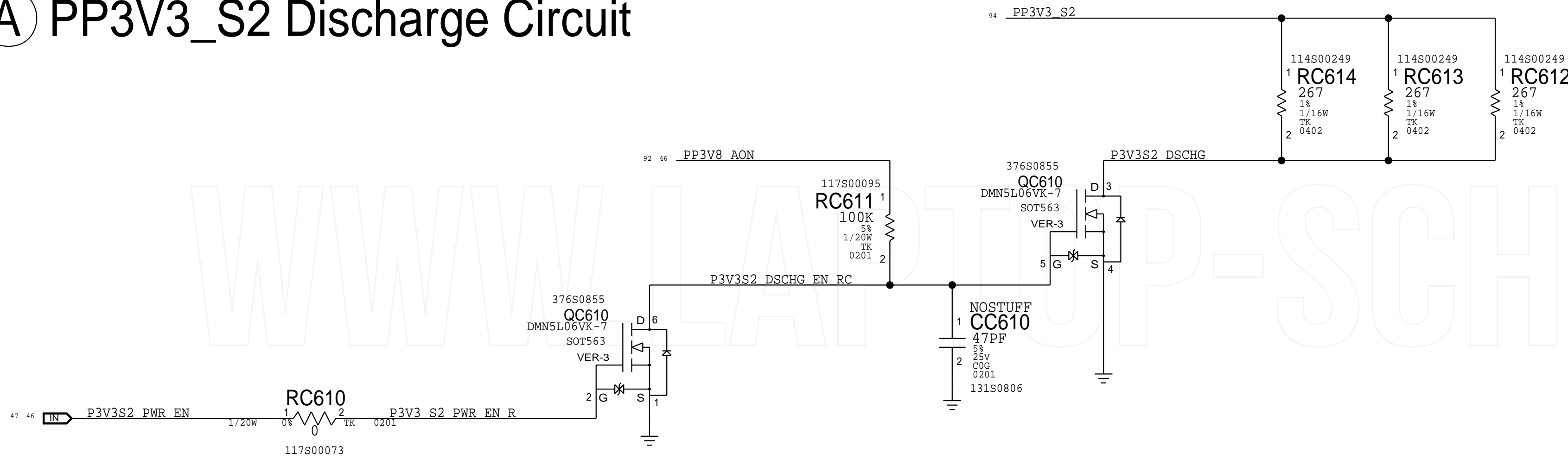
Vout=5.15V
EDC=6.6A
F=1.5MHz



POWER: 5V S2		
	DRAWING NUMBER	051-07020
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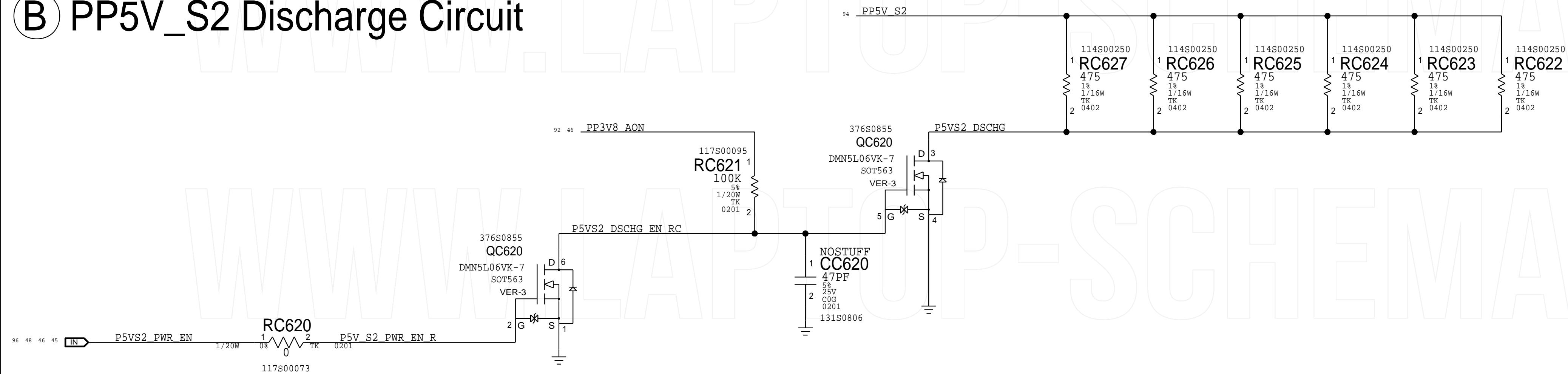
BOM_COST_GROUP=PLATFORM POWER

A PP3V3_S2 Discharge Circuit



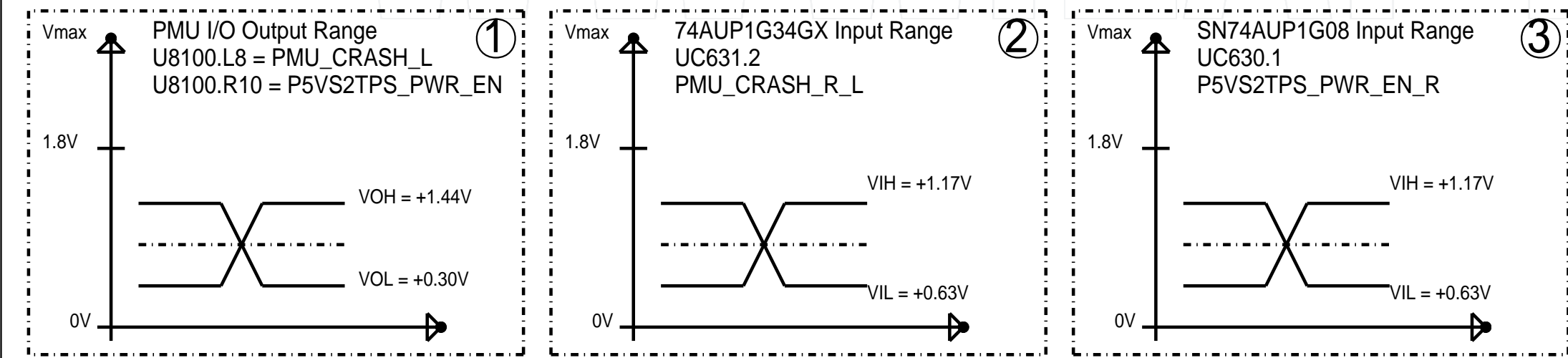
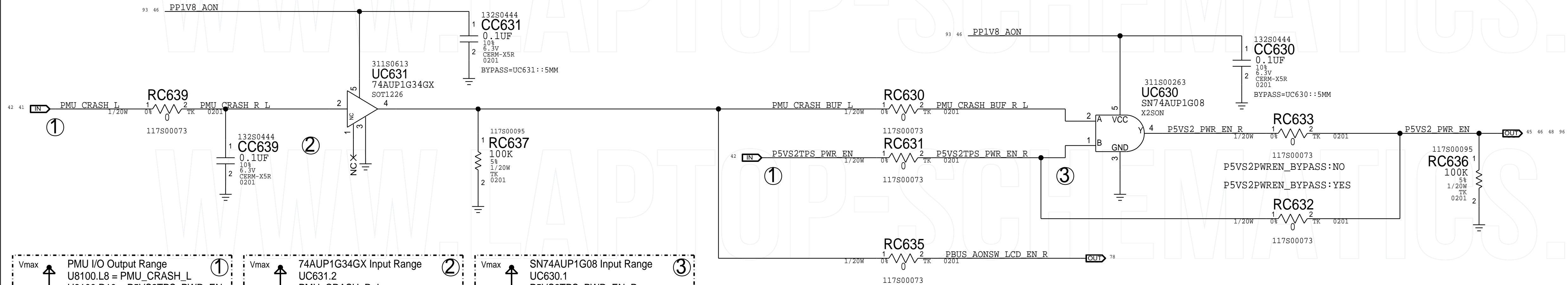
\$X2203GHUB/mlb/sim/ltspice/pp3v3_s2_discharge/pp3v3_s2_discharge_diodes_inc.asc

B PP5V_S2 Discharge Circuit

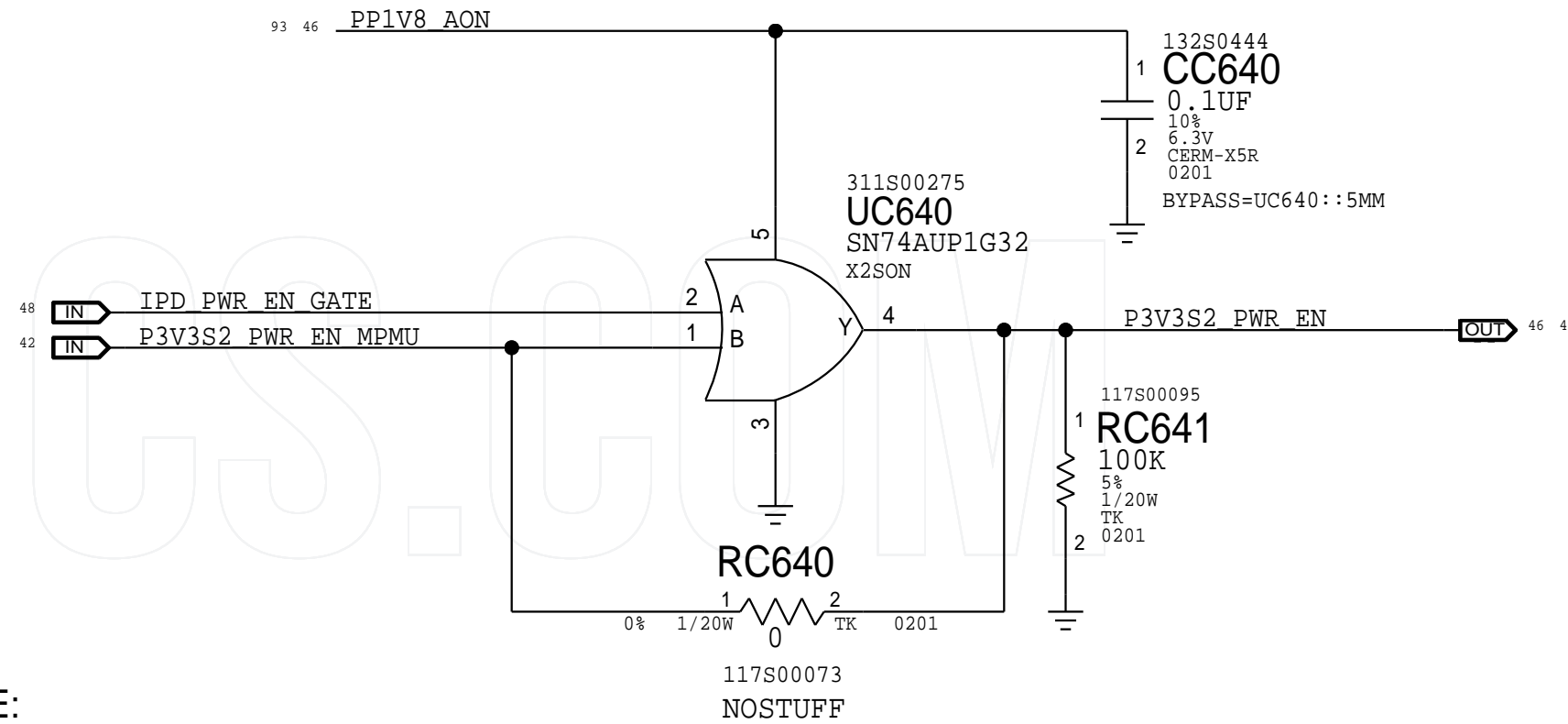


\$X2203GHUB/mlb/sim/ltspice/pp5v_s2_discharge/pp5v_s2_discharge_diodes_inc.asc

C P5VS2_PWR_EN Control Logic



D P3V3S2_PWR_EN Control Logic



NOTE:
Per Stowe PMU OTP, GPIO11 is OFF when the System is OFF.
A side-effect is that during the SIP_SMC->AWAKE transition the rail goes from ON->OFF->ON, which means we lose trackpad power during the OFF transition.
IPD_PWR_EN and PP5VS2_PWR_EN were moved to GPIOs that Stowe PMU can hold off.

POWER: 5V, 3V3 Support		
	DRAWING NUMBER	051-07020
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* OK2INTEGRATE *

3V3_S2 VR

SET ONE OPTION FOR PBUS CAPS

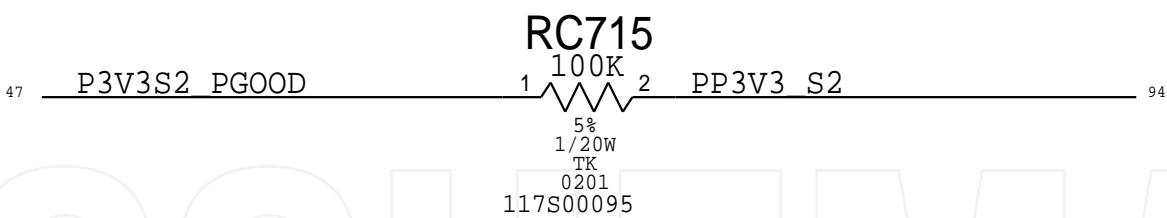
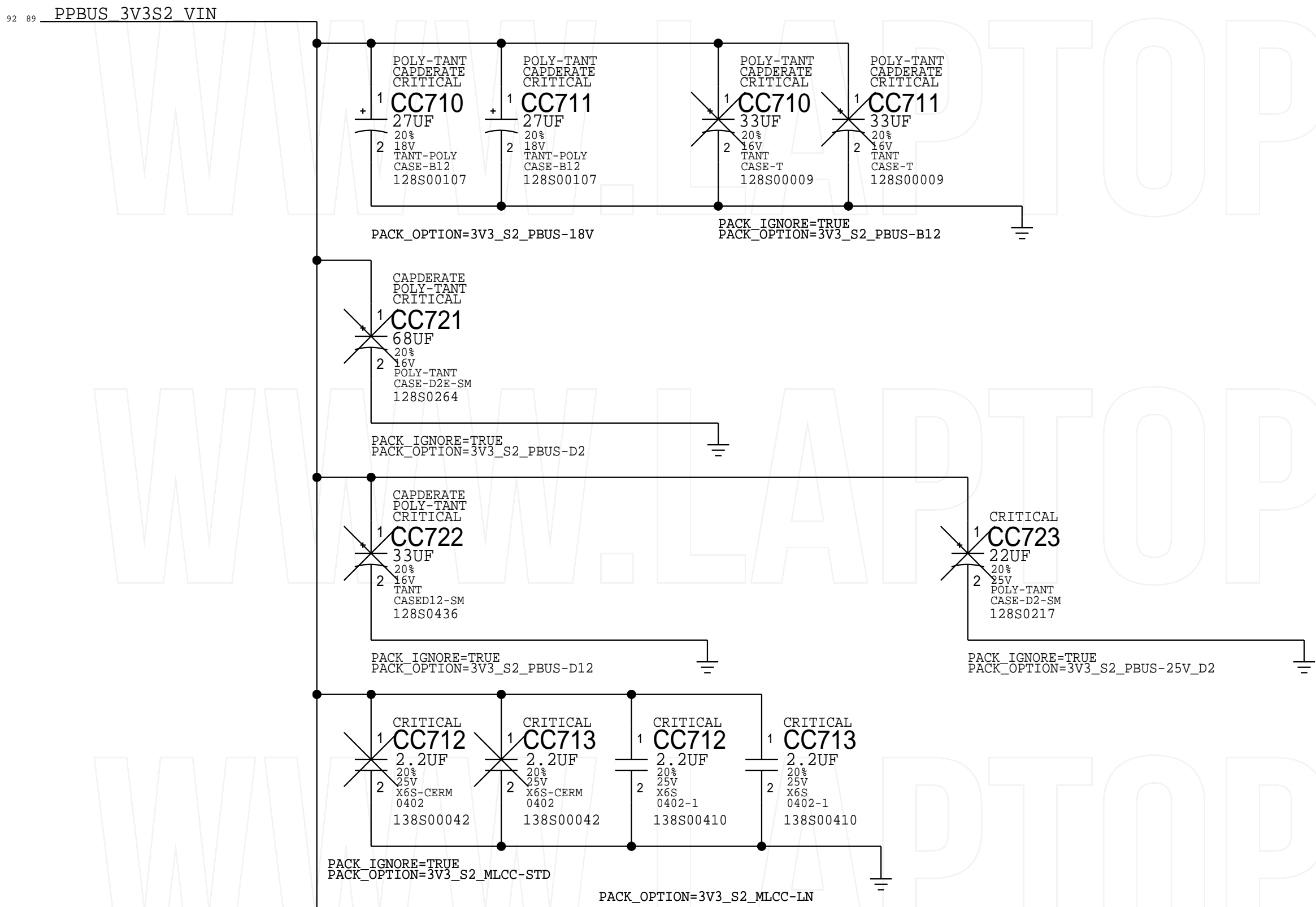
- PACK_OPTION=3V3_S2_PBUS-18V
- PACK_OPTION=3V3_S2_PBUS-B12
- PACK_OPTION=3V3_S2_PBUS-D2
- PACK_OPTION=3V3_S2_PBUS-D12
- PACK_OPTION=3V3_S2_PBUS-25V_D2

SET ONE OPTION FOR THE OUTPUT POLY CAPS

- PACK_OPTION=3V3_S2_VOUT-B2
- PACK_OPTION=3V3_S2_VOUT-B12

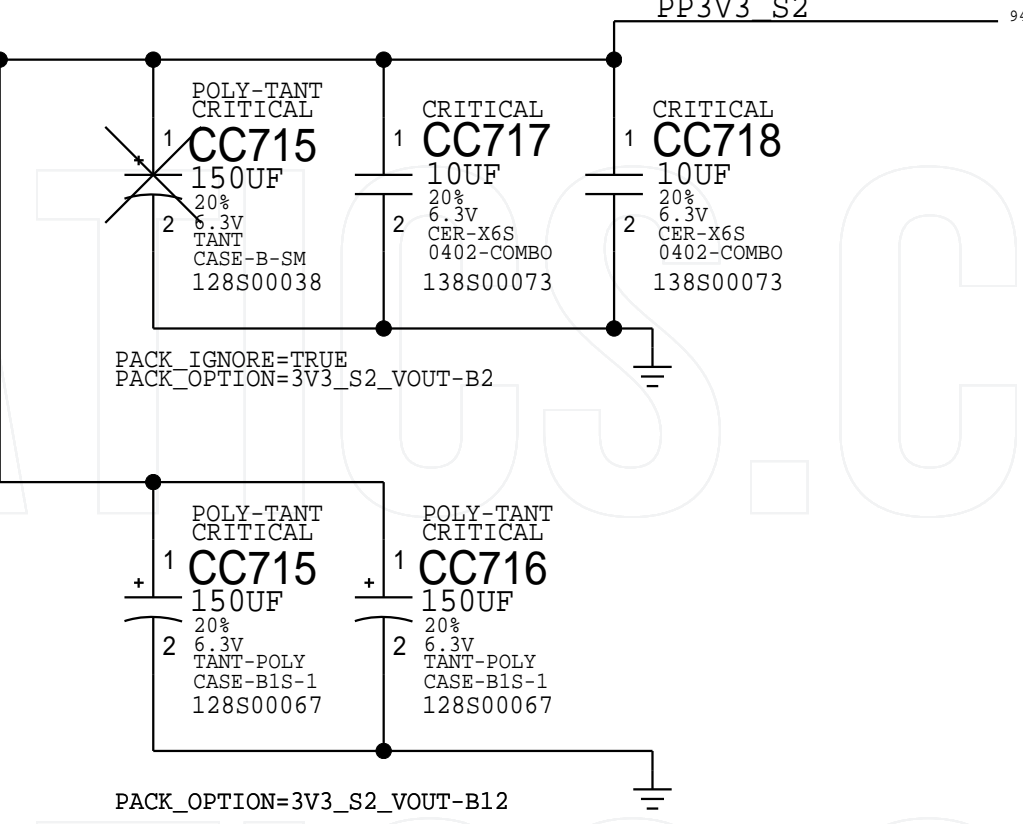
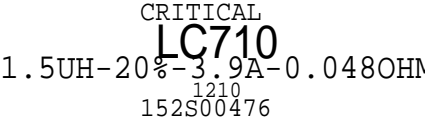
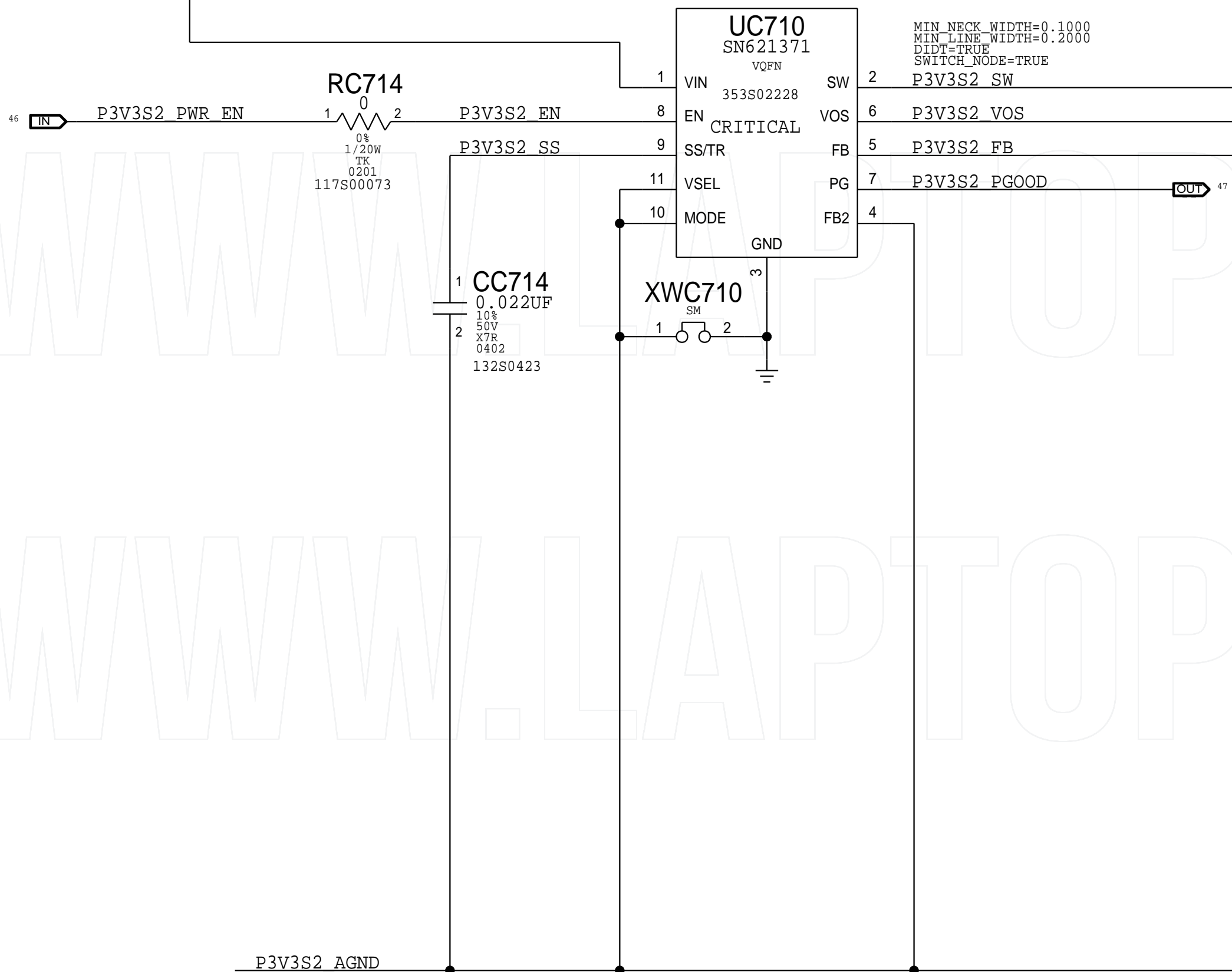
SET ONE OPTION FOR MLCC CAPS

- PACK_OPTION=3V3_S2_MLCC-STD
- PACK_OPTION=3V3_S2_MLCC-LN



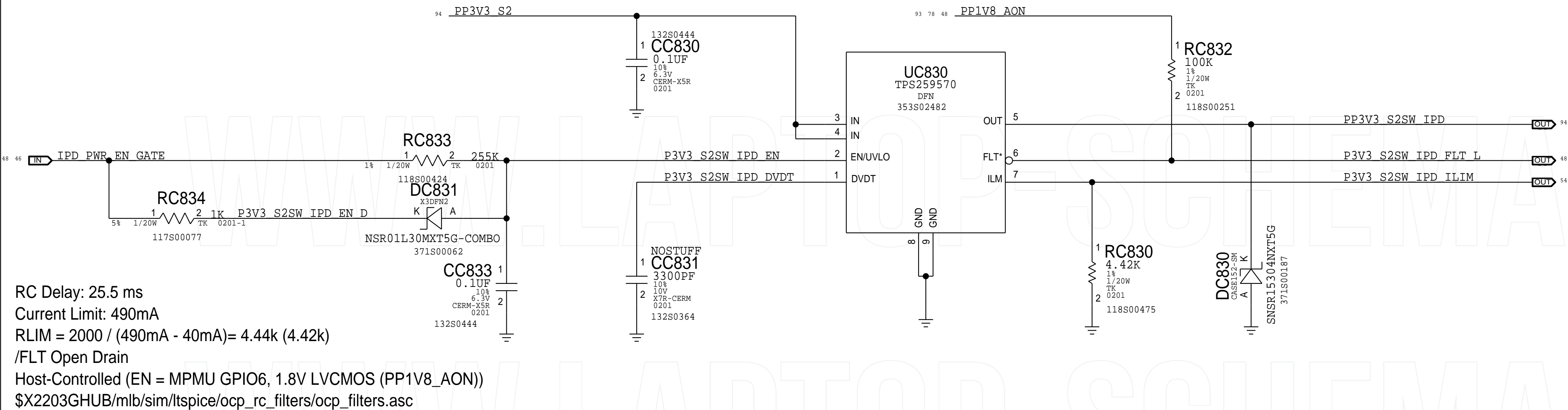
Startup time
min=4.3ms
typ=6.4ms
max=8.81ms

VOUT=3.3V
EDC=2.5A
TDC=2.5A
F=1.5MHz

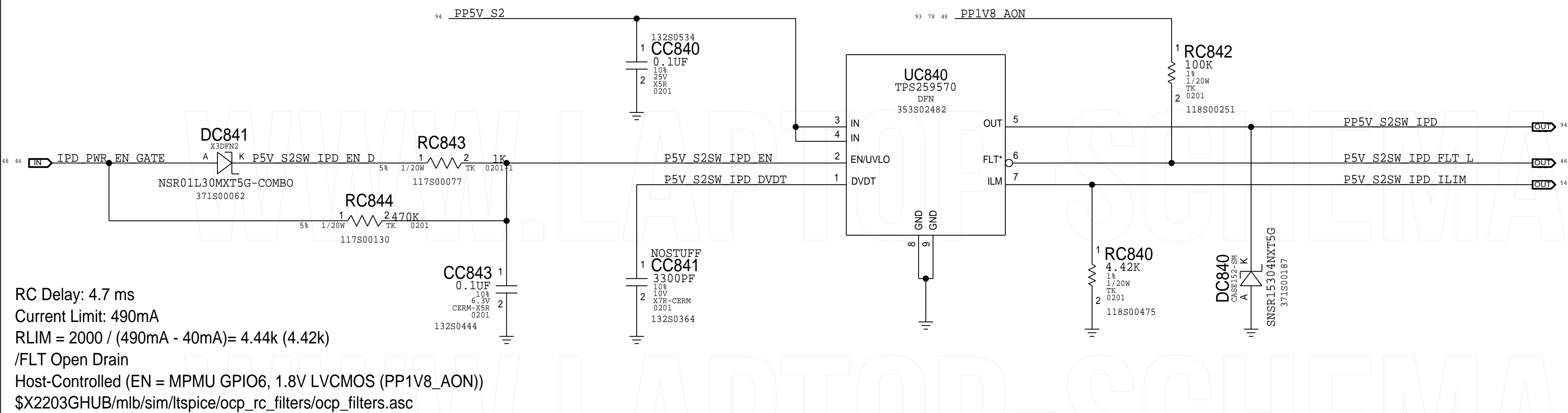


POWER: 3V3 S2		
	DRAWING NUMBER	051-07020
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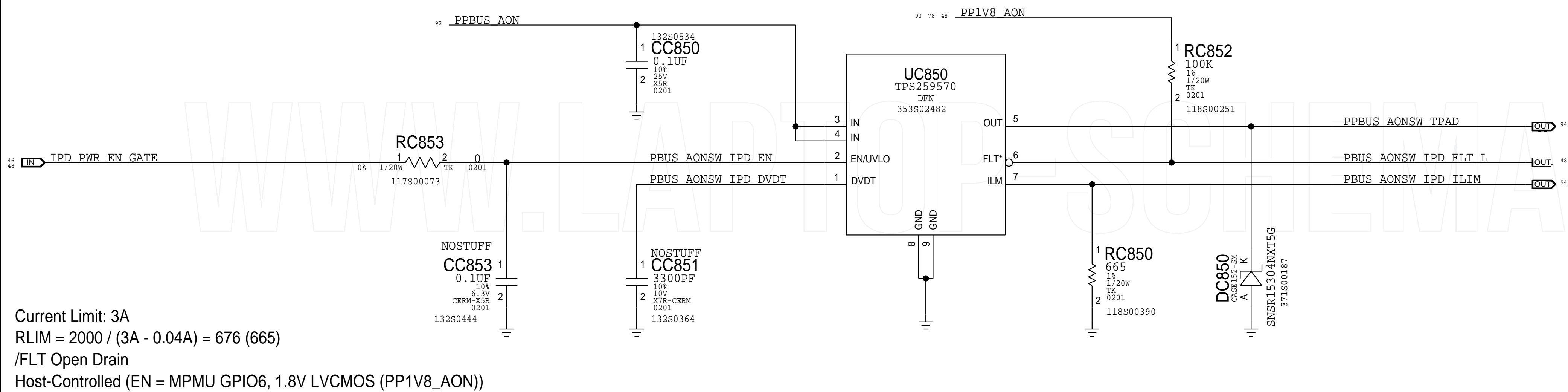
A PP3V3_S2SW_IPD Load Switch & e-Fuse



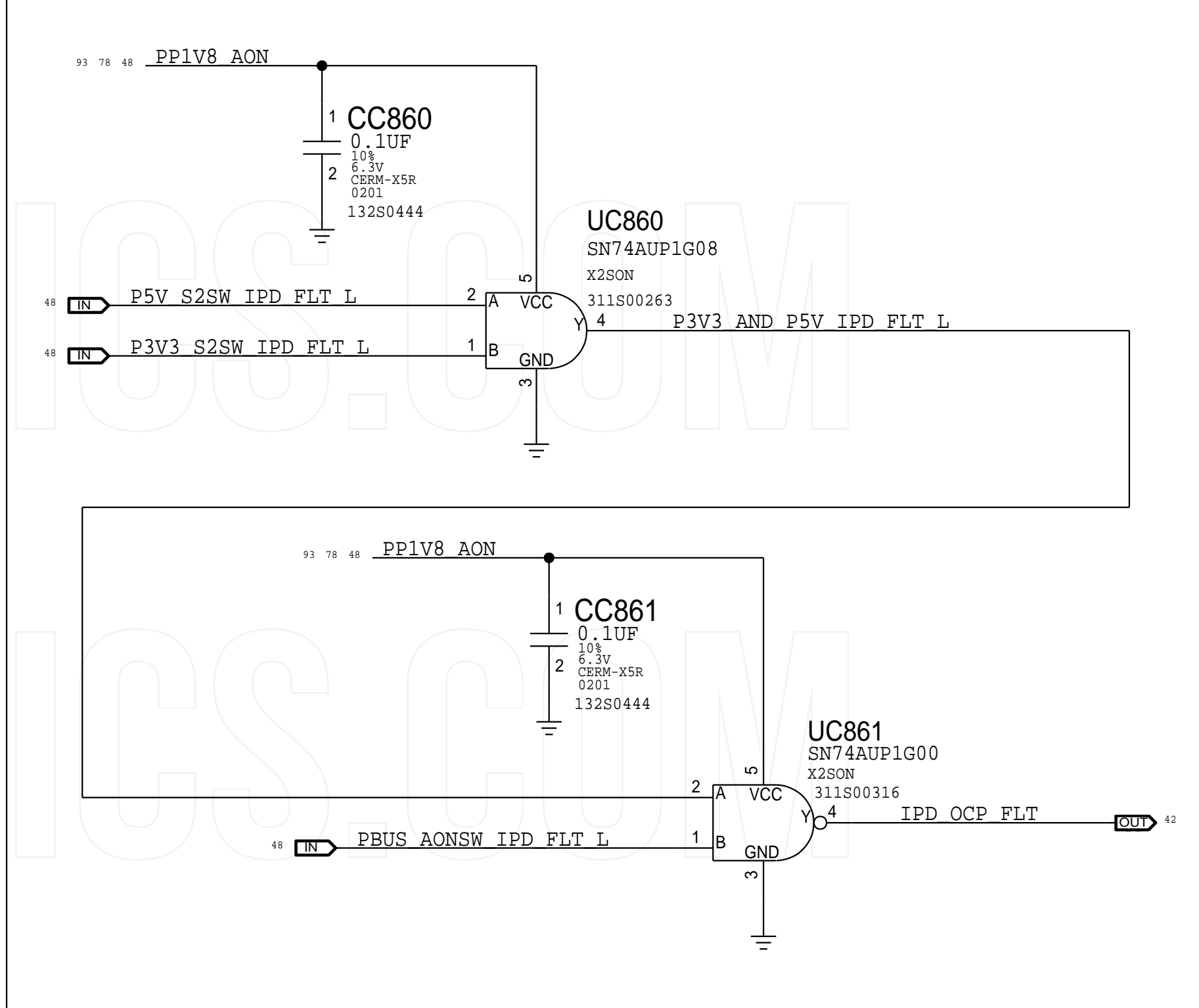
B PP5V_S2SW_IPD Load Switch & e-Fuse



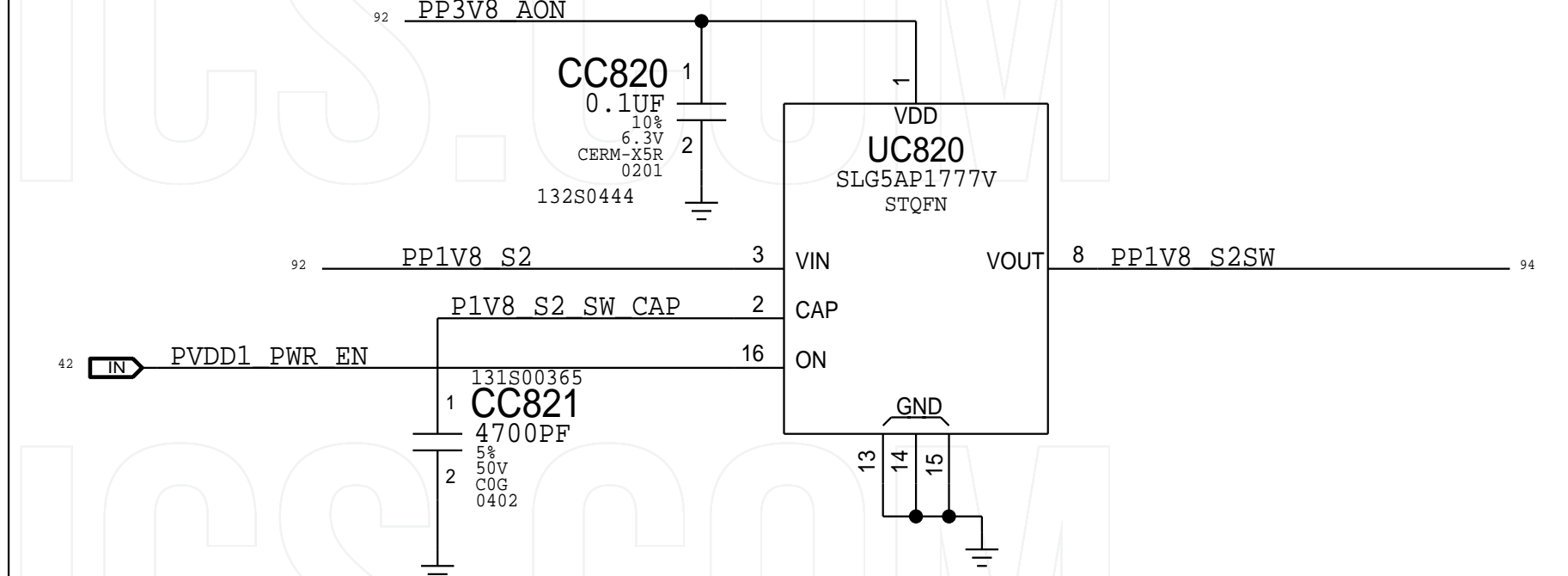
C PPBUS_AONSW_IPD Load Switch & e-Fuse



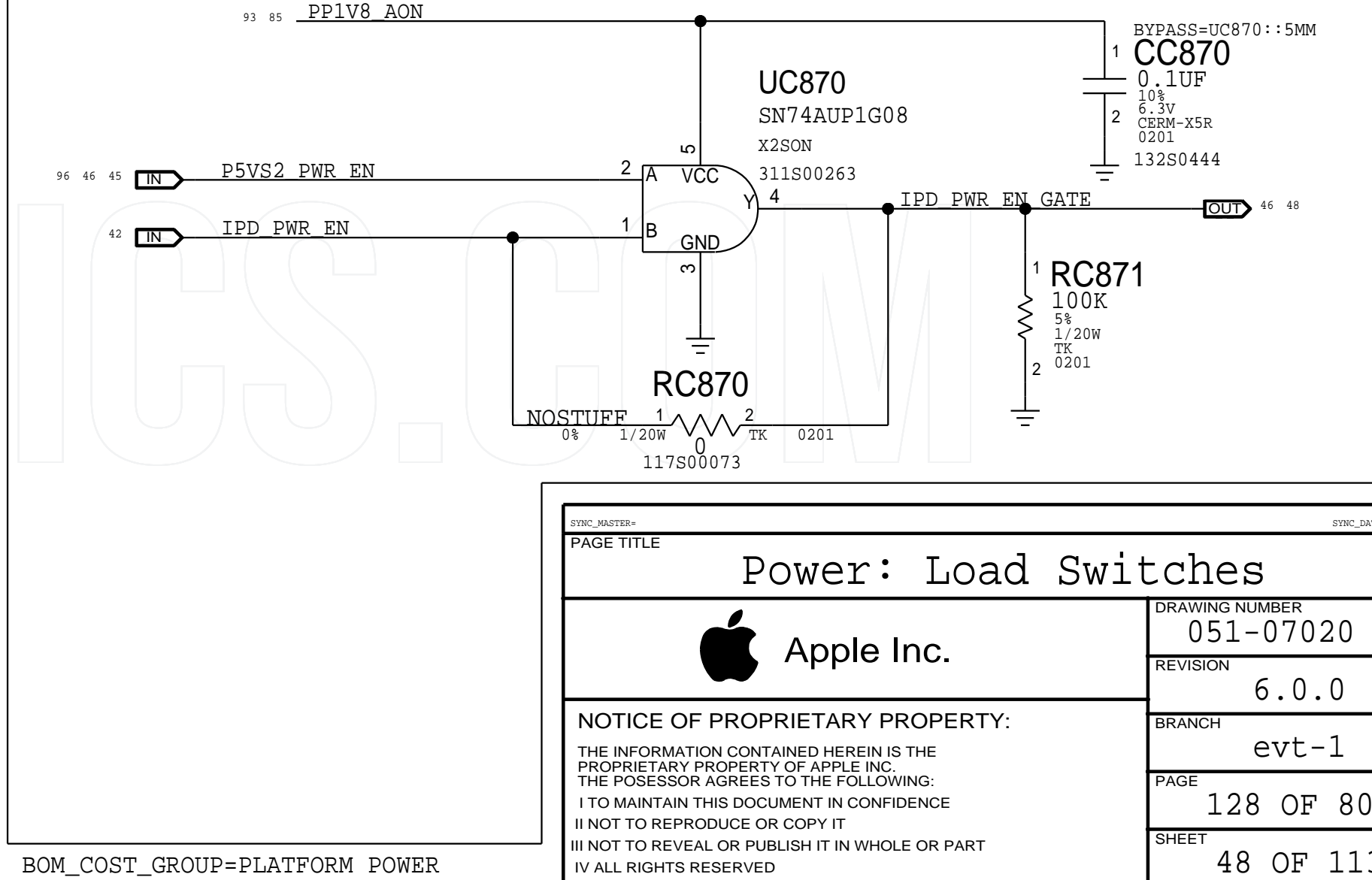
C IPD_OCP_FLT Control Logic



E PP1V8_S2SW Load Switch



F IPD_PWR_EN Gating Logic

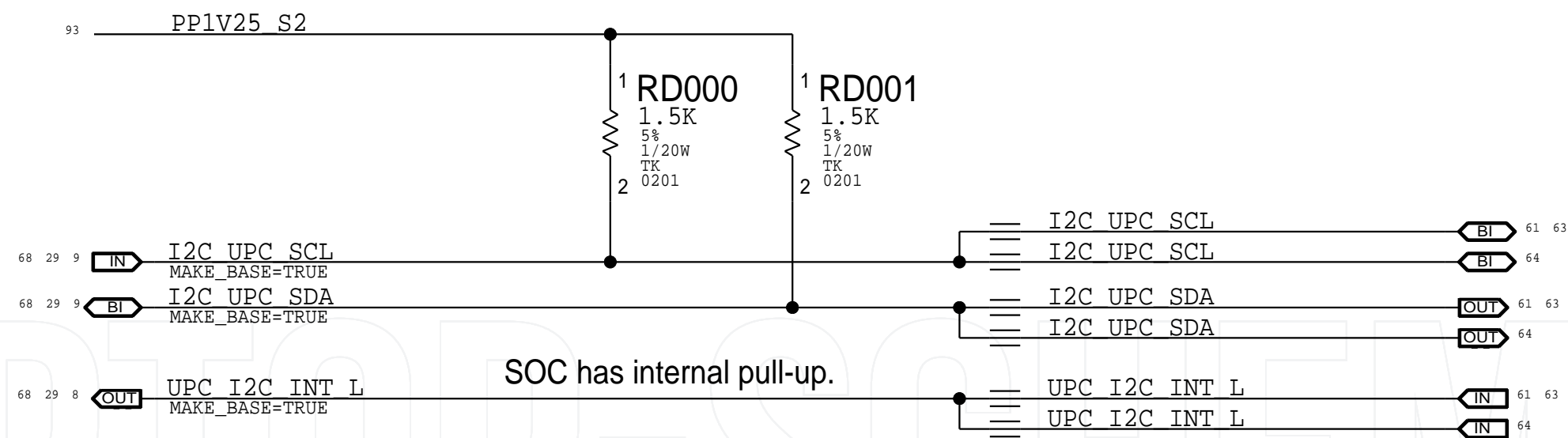


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Power: Load Switches			051-07020		
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BOM_COST_GROUP=PLATFORM POWER

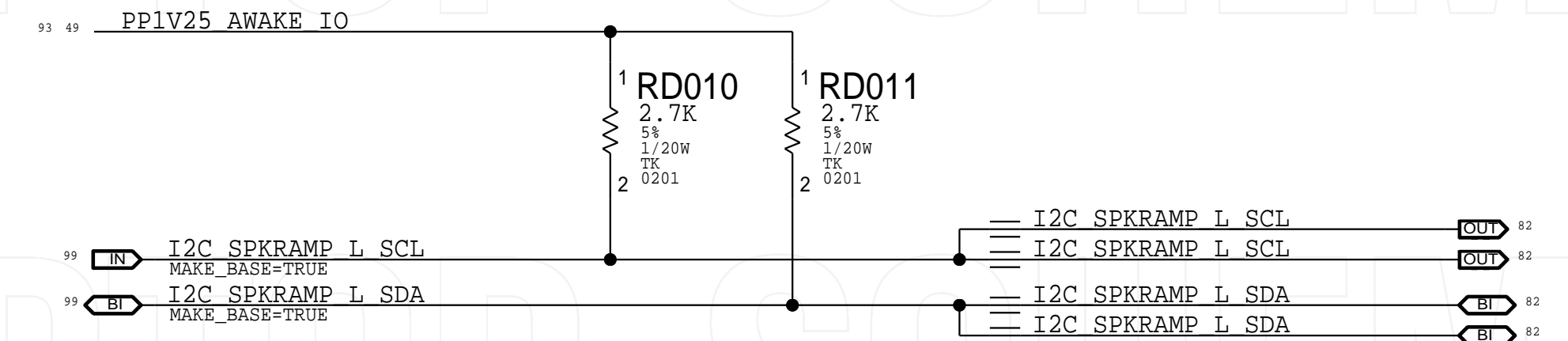
A AP_I2C0 - I2C Interface

MASTER	NUMBER	SPEED	7-BIT ADDR	8-BIT ADDR (R)	DEVICE
AP	0	400 kHz	0X38	0X71	ACE2 - 0
AP	0	400 kHz	0X3F	0X7F	ACE2 - 1
AP	0	400 kHz	0X3A	0X75	ACE2 - MagSafe



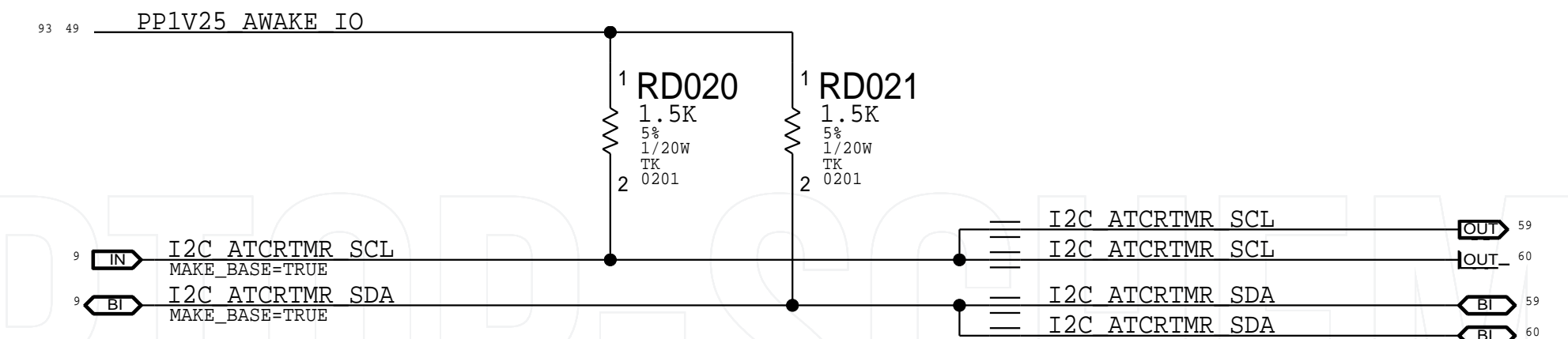
B AP_I2C1 - I2C Interface

MASTER	NUMBER	SPEED	7-BIT ADDR	8-BIT ADDR (R)	DEVICE
AP	1	400 kHz	0X38	0X71	Left SpkrAmp A
AP	1	400 kHz	0X39	0X73	Left SpkrAmp B



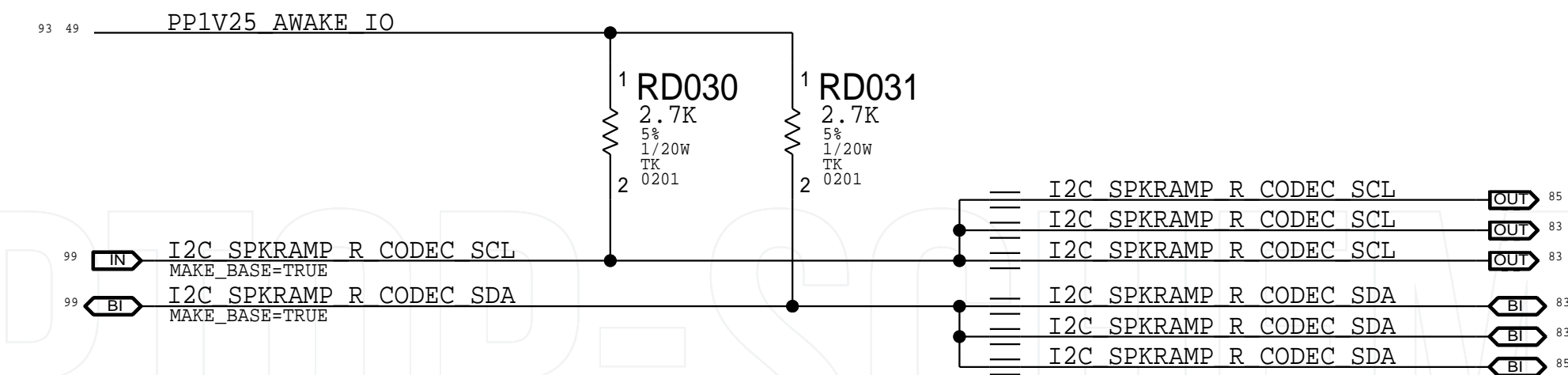
C AP_I2C2 - I2C Interface

MASTER	NUMBER	SPEED	7-BIT ADDR	8-BIT ADDR (R)	DEVICE
AP	2	100 kHz/400 kHz	0X18	0X31	RT13 Port 0
AP	2	100 kHz/400 kHz	0X19	0X33	RT13 Port 1



D AP_I2C3 - I2C Interface

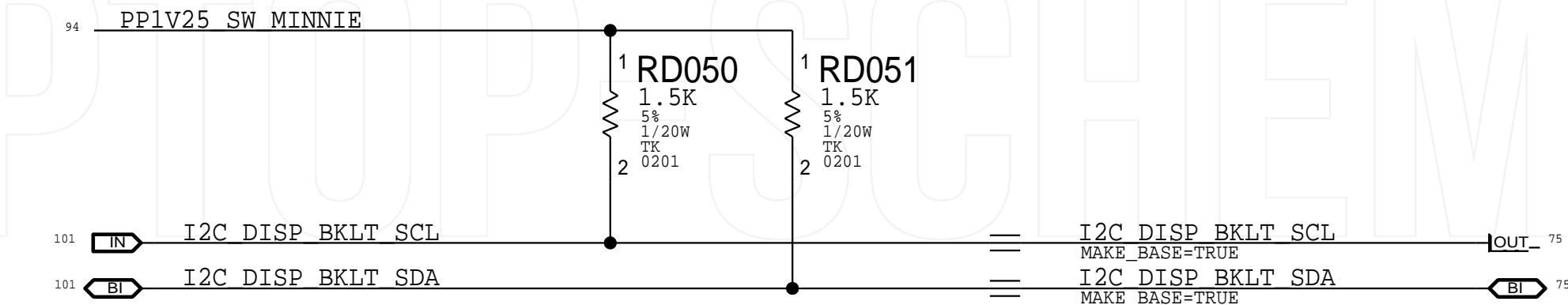
MASTER	NUMBER	SPEED	7-BIT ADDR	8-BIT ADDR (R)	DEVICE
AP	3	400 kHz	0X3B	0X77	Right SpkrAmp D
AP	3	400 kHz	0X3C	0X79	Right SpkrAmp E
AP	3	400 kHz	0X4B	0X97	CODEC



E AP_I2C4 - I2C Interface (Unused)

F DISP_I2C - I2C Interface

MASTER	NUMBER	SPEED	7-BIT ADDR	8-BIT ADDR (R)	DEVICE
DISP	0	100 kHz	0X2F	0X5F	Minnie Bklt Drvr

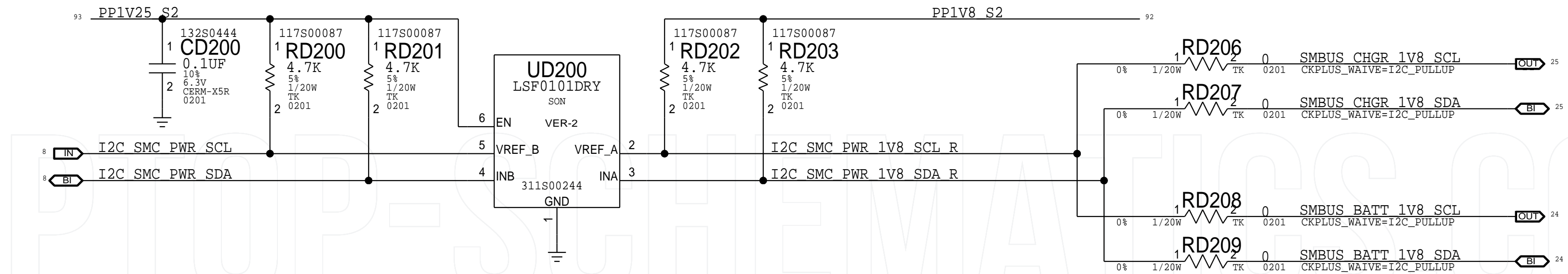


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I2C: AP, DISP			051-07020		
Apple Inc.			REVISION		
			6.0.0		
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BOM_COST_GROUP=SENSORS

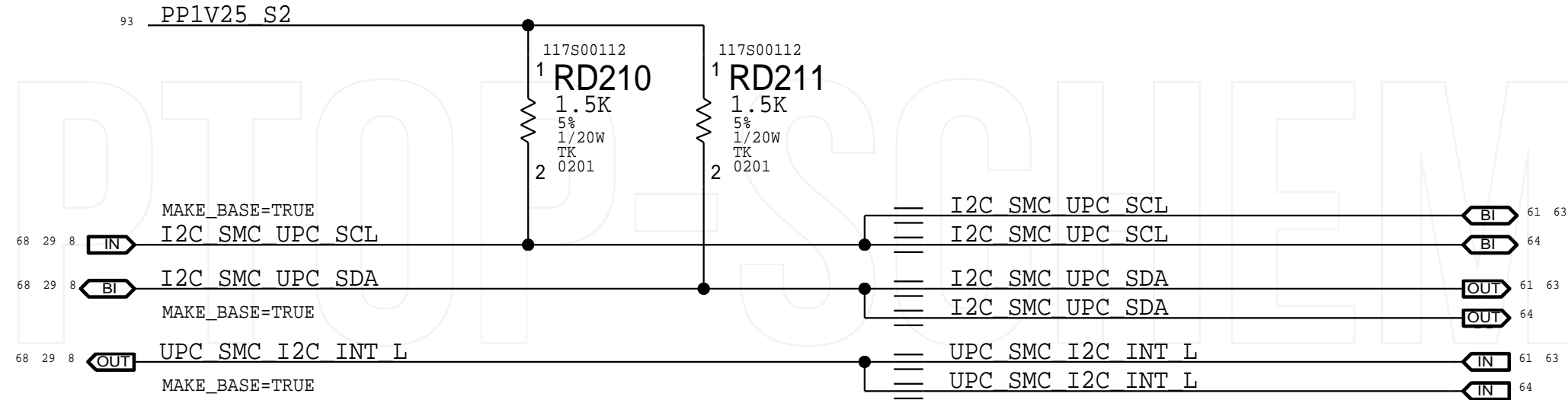
A SMC_I2C0 - I2C Interface

MASTER	NUMBER	SPEED	7-BIT ADDR	8-BIT ADDR (R)	DEVICE
SMC	0	100 kHz	0X09	0X13	Whamola Charger
SMC	0	100 kHz	0X0B	0X16	Battery BMU
SMC	0	100 kHz	0X40	0X81	INA233 - U202
SMC	0	100 kHz	0X44	0X89	INA233 - U203
SMC	0	100 kHz	0X45	0X8B	INA233 - U201



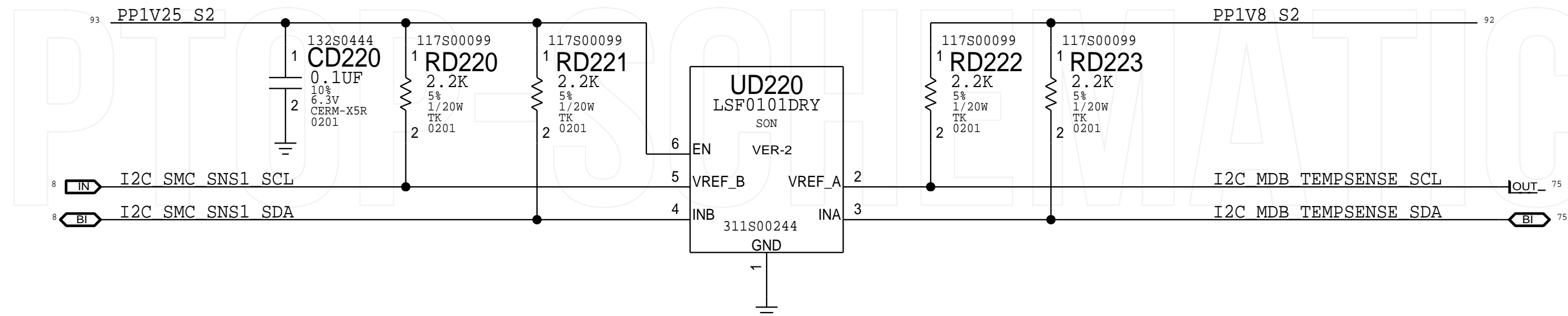
B SMC_I2C1 - I2C Interface

MASTER	NUMBER	SPEED	7-BIT ADDR	8-BIT ADDR (R)	DEVICE
SMC	1	400 kHz	0X38	0X71	ACE2 - 0
SMC	1	400 kHz	0X3F	0X7F	ACE2 - 1
SMC	1	400 kHz	0X3A	0X75	ACE2 - MagSafe



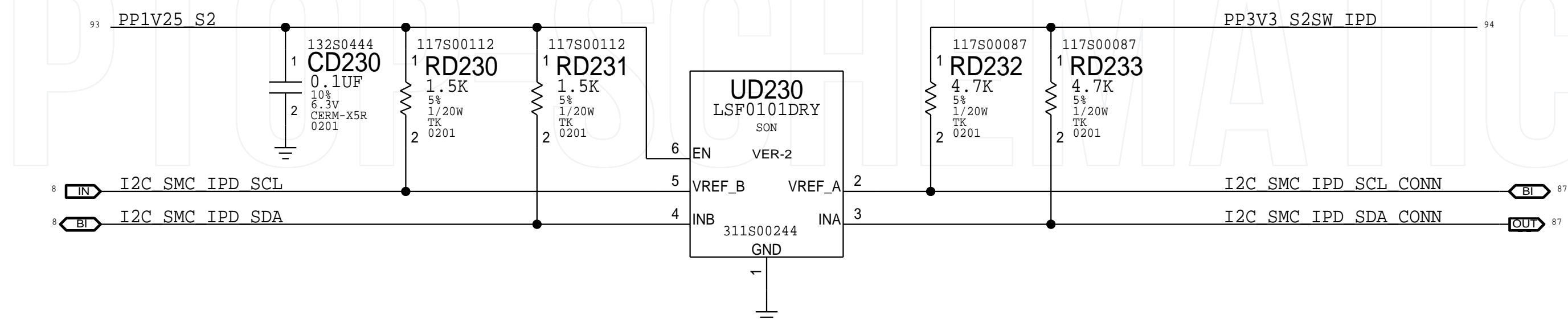
C SMC_I2C2 - I2C Interface

MASTER	NUMBER	SPEED	7-BIT ADDR	8-BIT ADDR (R)	DEVICE
SMC	2	100 kHz	0X48	0X91	MDB - TMP468

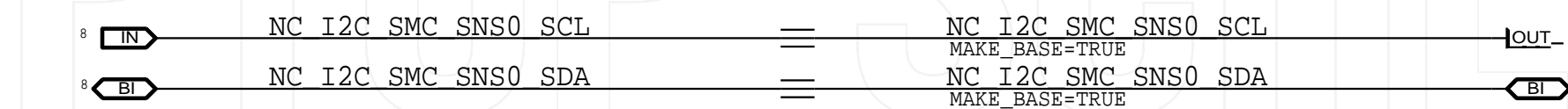


D SMC_I2C3 - I2C Interface

MASTER	NUMBER	SPEED	7-BIT ADDR	8-BIT ADDR (R)	DEVICE
SMC	3	100 kHz	0X4C	0X99	PAIM - TempSense



E SMC_I2C4 - I2C Interface (Unused)

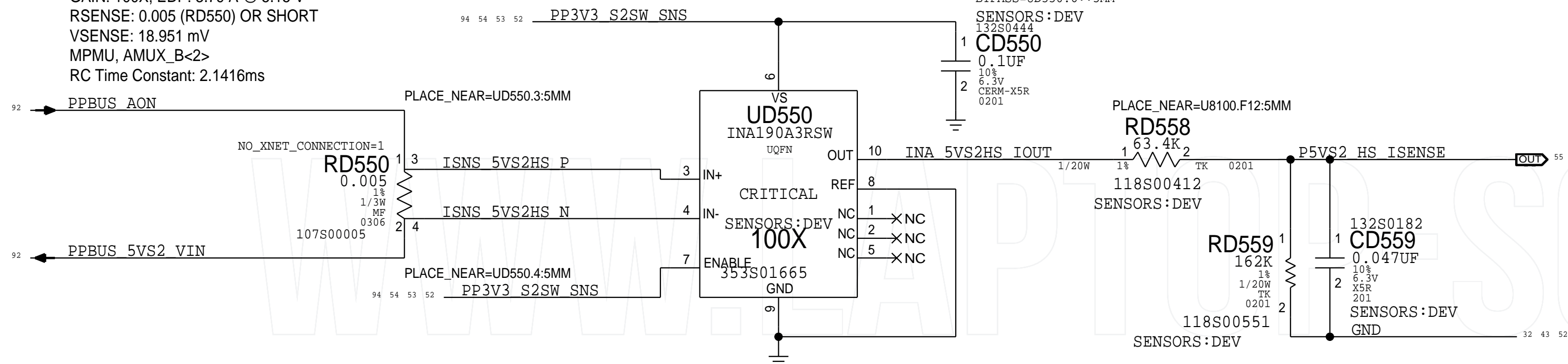


PAGE TITLE			I2C: SMC		
			DRAWING NUMBER	051-07020	SIZE
			REVISION	6.0.0	D
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			PAGE	132 OF 801	
			SHEET	51 OF 113	

BOM_COST_GROUP=SENSORS

A 5V S2 VR High Side Current Sensor (IO5R)

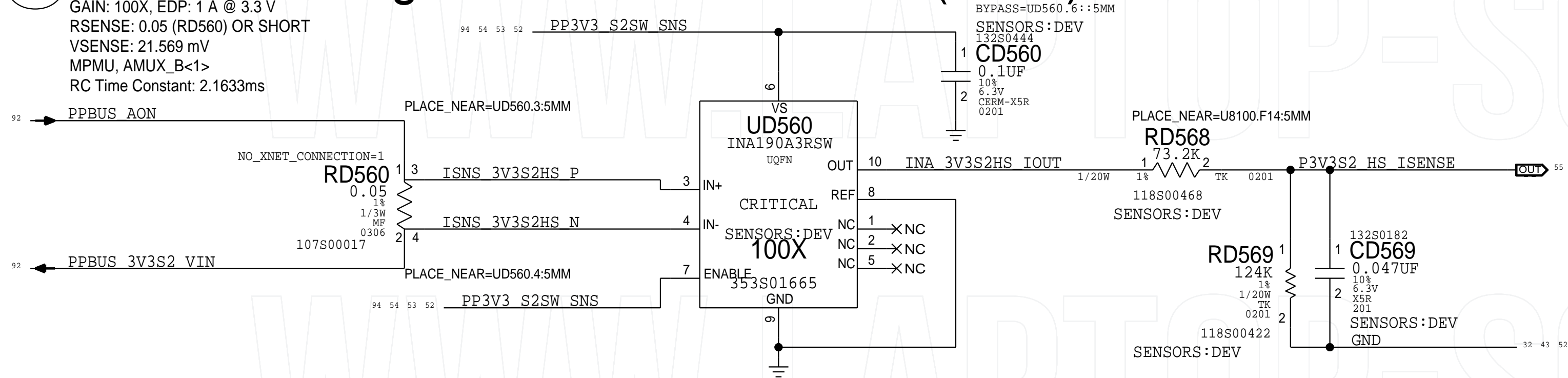
GAIN: 100X, EDP: 3.79 A @ 5.15 V
RSENSE: 0.005 (RD550) OR SHORT
VSENSE: 18.951 mV
MPMU, AMUX_B<2>
RC Time Constant: 2.1416ms



\$X2203GHUB/mlb/sim/ltspice/io5r_p5vs2_hs_isense/io5r_p5vs2_hs_isense.asc

B 3V3 S2 VR High Side Current Sensor (IO3R)

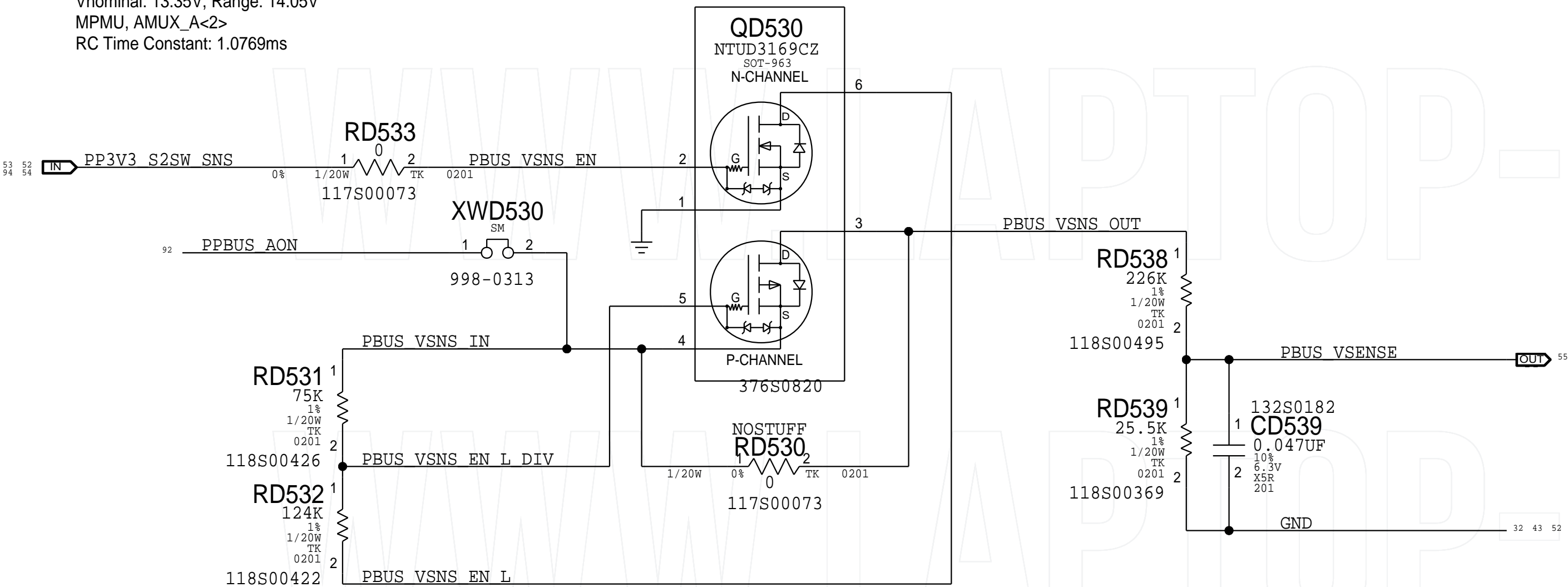
GAIN: 100X, EDP: 1 A @ 3.3 V
RSENSE: 0.05 (RD560) OR SHORT
VSENSE: 21.569 mV
MPMU, AMUX_B<1>
RC Time Constant: 2.1633ms



\$X2203GHUB/mlb/sim/ltspice/io3r_p3v3s2_hs_isense/io3r_p3v3s2_hs_isense.asc

C PPBUS Voltage Sensor (VP0R)

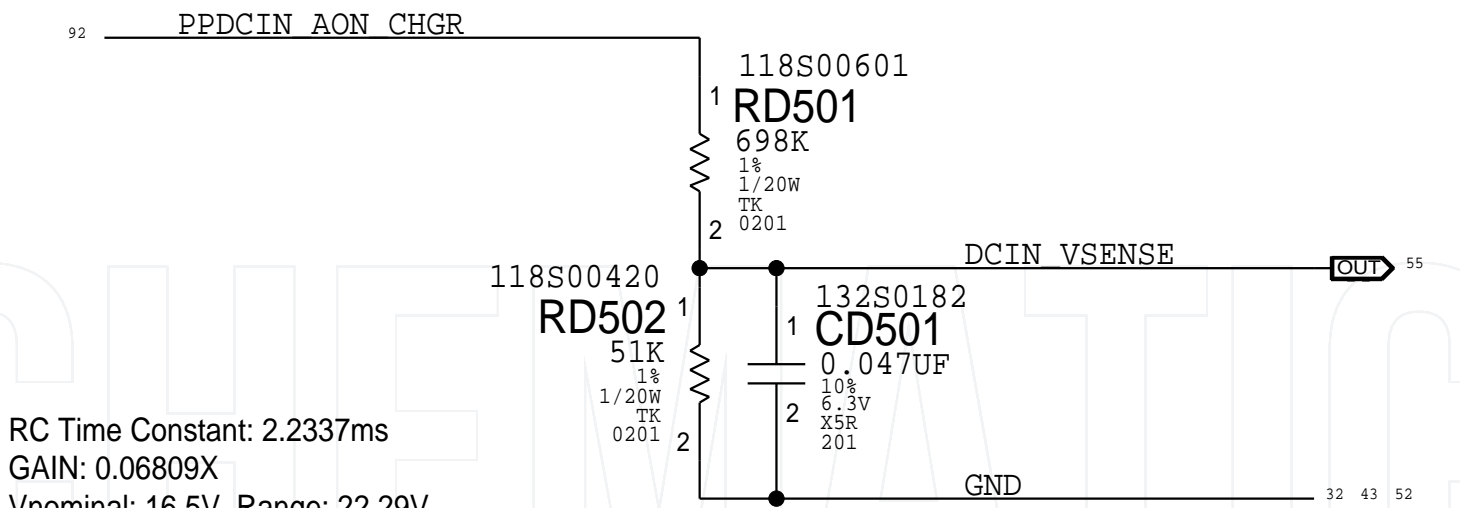
GAIN: 0.1014X
Vnominal: 13.35V, Range: 14.05V
MPMU, AMUX_A<2>
RC Time Constant: 1.0769ms



\$X2203GHUB/mlb/sim/ltspice/vp0r_sense/vp0r_pbus_vsense_pulse_diodesinc.asc
\$X2203GHUB/mlb/sim/ltspice/vp0r_sense/vp0r_pbus_vsense_pulse_onsemi.asc

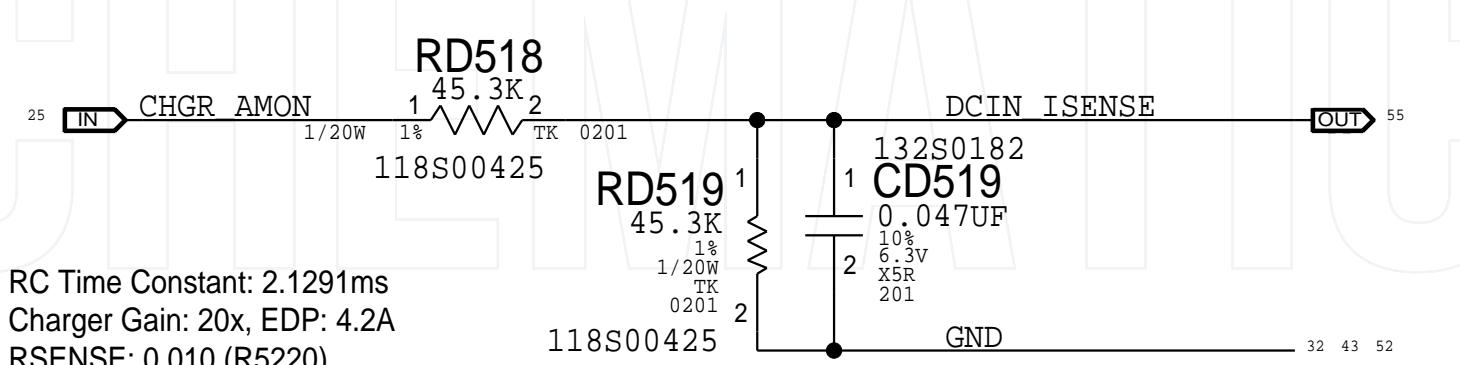
D DCIN Voltage Sensor (VD0R)

RC Time Constant: 2.2337ms
GAIN: 0.06809X
Vnominal: 16.5V, Range: 22.29V
MPMU, AMUX_A<0>



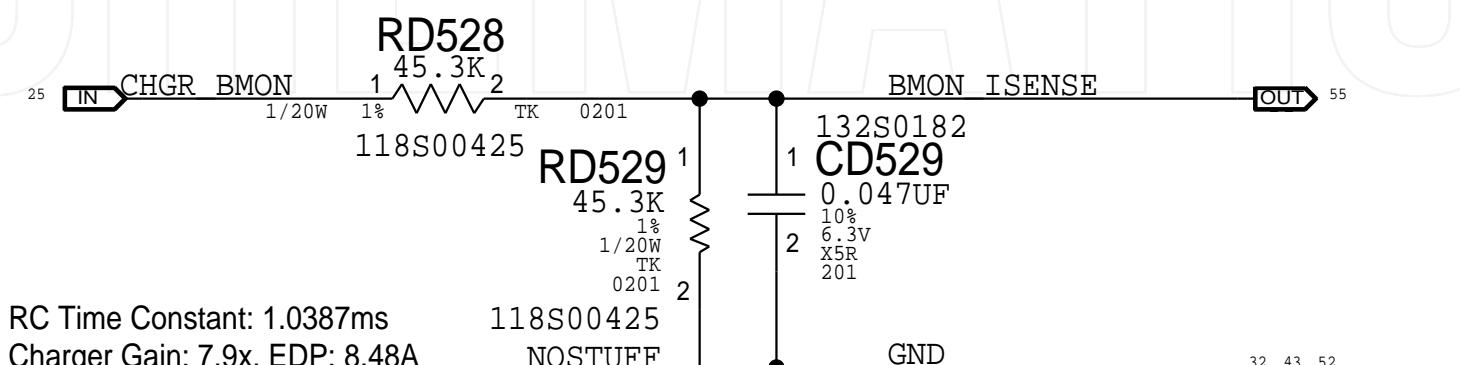
E DCIN Current Sensor (ID0R)

RC Time Constant: 2.1291ms
Charger Gain: 20x, EDP: 4.2A
RSENSE: 0.010 (R5220)
MPMU, AMUX_A<1>



F BMON Current Sensor (IPBR)

RC Time Constant: 1.0387ms
Charger Gain: 7.9x, EDP: 8.48A
RSENSE: 0.005 (R5260)
MPMU, AMUX_A<3>



G Production Sensor BOM Table

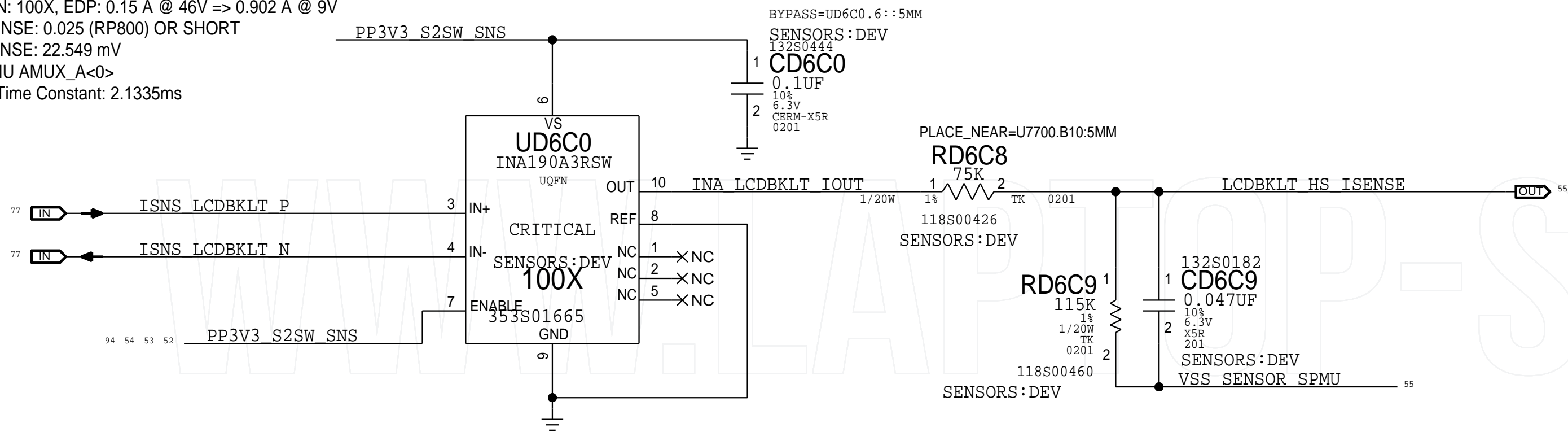
PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
117S00095	1	RES,TK,100K OHM,5%,1/20W,0201	RD559		SENSORS:PROD
117S00095	1	RES,TK,100K OHM,5%,1/20W,0201	RD569		SENSORS:PROD

PAGE TITLE		
SENSORS: POWER HIGH SIDE (1/2)		
	DRAWING NUMBER	051-07020
	REVISION	6.0.0
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BOM_COST_GROUP=SENSORS

A LCD Backlight High Side Current Sensor (IBLR)

GAIN: 100X, EDP: 0.15 A @ 46V => 0.902 A @ 9V
RSENSE: 0.025 (RP800) OR SHORT
VSENSE: 22.549 mV
SPMU AMUX_A<0>
RC Time Constant: 2.1335ms

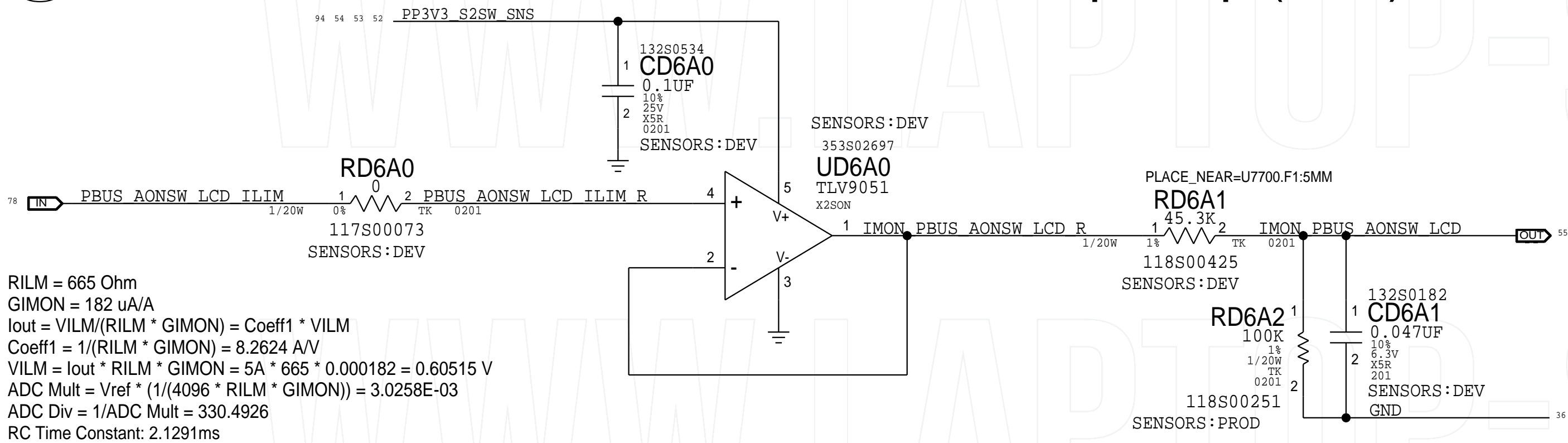


\$X2203GHUB/mlb/sim/ltspice/iblr_lcdbklt_hs_isense/iblr_lcdbklt_hs_isense.asc

C Production Sensor BOM Table

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
117800095	1	RES, TK, 100K OHM, 5%, 1/20W, 0201	RD6C9		SENSORS: PROD

B PPBUS_AONSW_LCD Current Sense Op-Amp (IBIR)



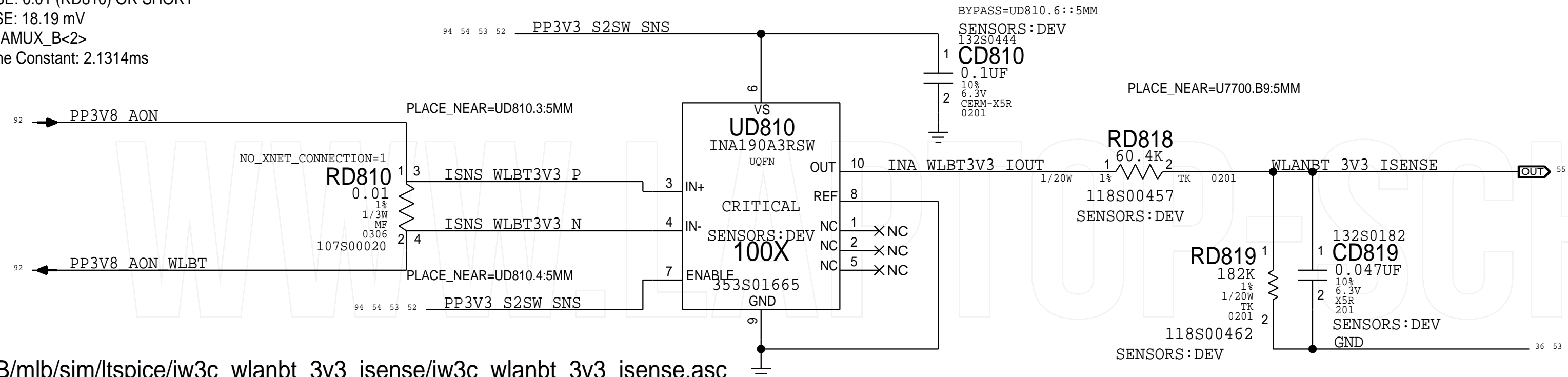
RILM = 665 Ohm
GIMON = 182 uA/A
Iout = VILM/(RILM * GIMON) = Coeff1 * VILM
Coeff1 = 1/(RILM * GIMON) = 8.2624 A/V
VILM = Iout * RILM * GIMON = 5A * 665 * 0.000182 = 0.60515 V
ADC Mult = Vref * (1/(4096 * RILM * GIMON)) = 3.0258E-03
ADC Div = 1/ADC Mult = 330.4926
RC Time Constant: 2.1291ms

PAGE TITLE		
SENSORS: POWER HIGH SIDE (2/2)		
	DRAWING NUMBER	051-07020
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BOM_COST_GROUP=SENSORS

A WLAN BT 3V8 AON Current Sensor (IW3C)

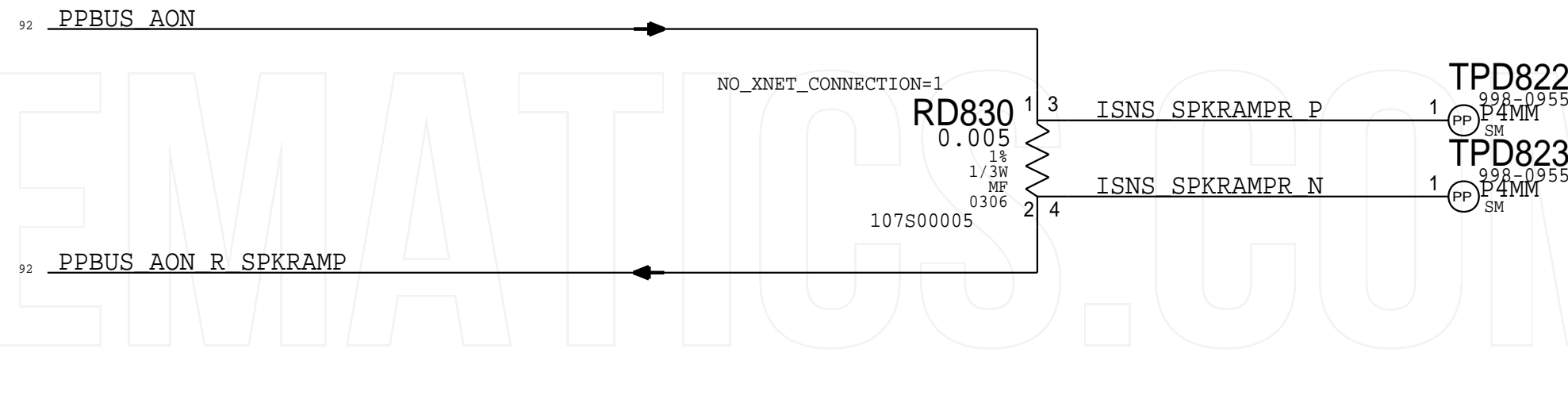
GAIN: 100X, EDP: 1.819 A @ 3.8 V
RSENSE: 0.01 (RD810) OR SHORT
VSENSE: 18.19 mV
SPMU AMUX_B<2>
RC Time Constant: 2.1314ms



\$X2203GHUB/mlb/sim/ltspice/iw3c_wlanbt_3v3_isense/iw3c_wlanbt_3v3_isense.asc

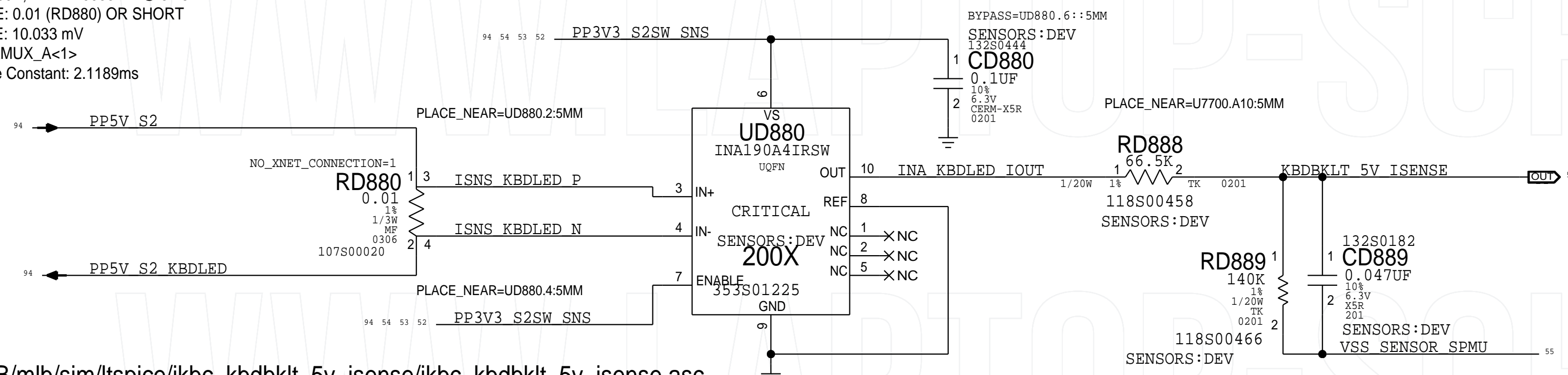
E Right Speaker Amplifier Current Sensor (Ixxx)

GAIN: 100X, EDP: 2.6 A
RSENSE: 0.005 (RD820) OR SHORT
VSENSE: 13 mV, RANGE: 3.3 A



B Keyboard LED 5V Current Sensor (IKBC)

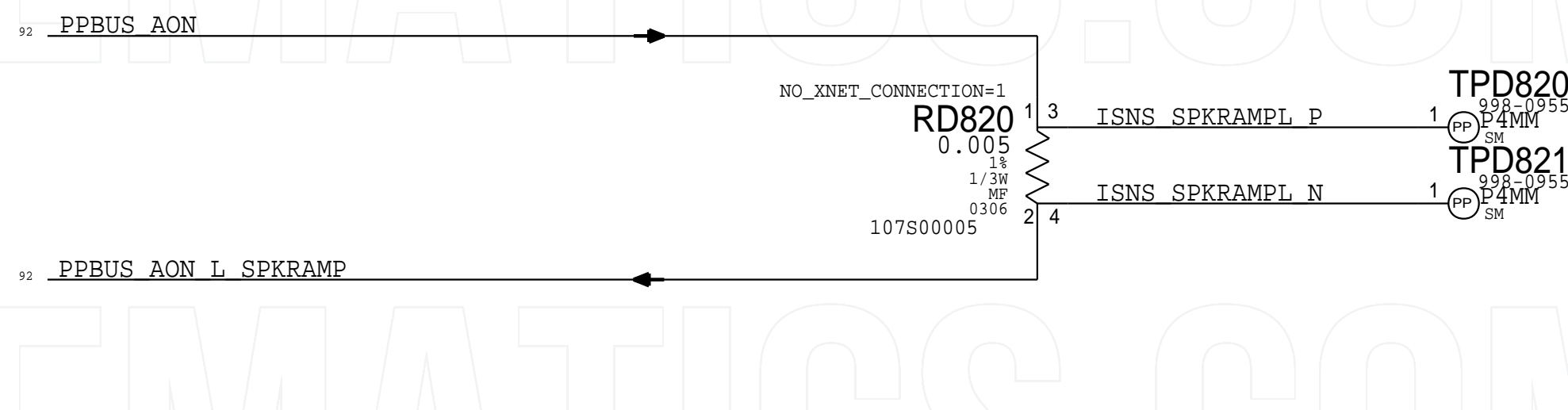
GAIN: 200X, EDP: 1.00331 A @ 5.15 V
RSENSE: 0.01 (RD880) OR SHORT
VSENSE: 10.033 mV
SPMU AMUX_A<1>
RC Time Constant: 2.1189ms



\$X2203GHUB/mlb/sim/ltspice/ikbc_kbdbklt_5v_isense/ikbc_kbdbklt_5v_isense.asc

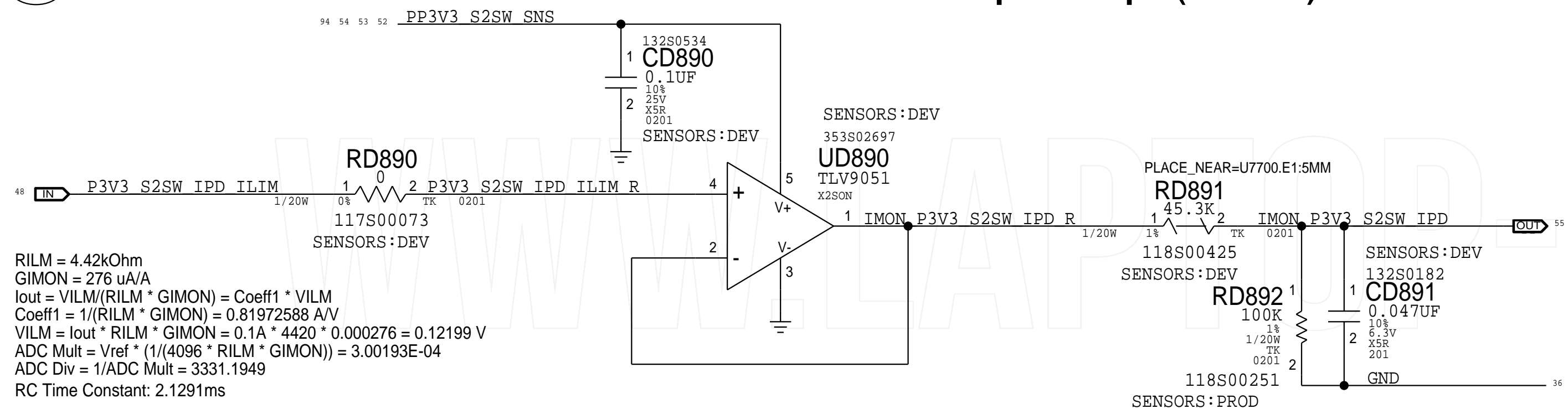
F Left Speaker Amplifier Current Sensor (Ixxx)

GAIN: 100X, EDP: 2.6 A
RSENSE: 0.005 (RD820) OR SHORT
VSENSE: 13 mV, RANGE: 3.3 A



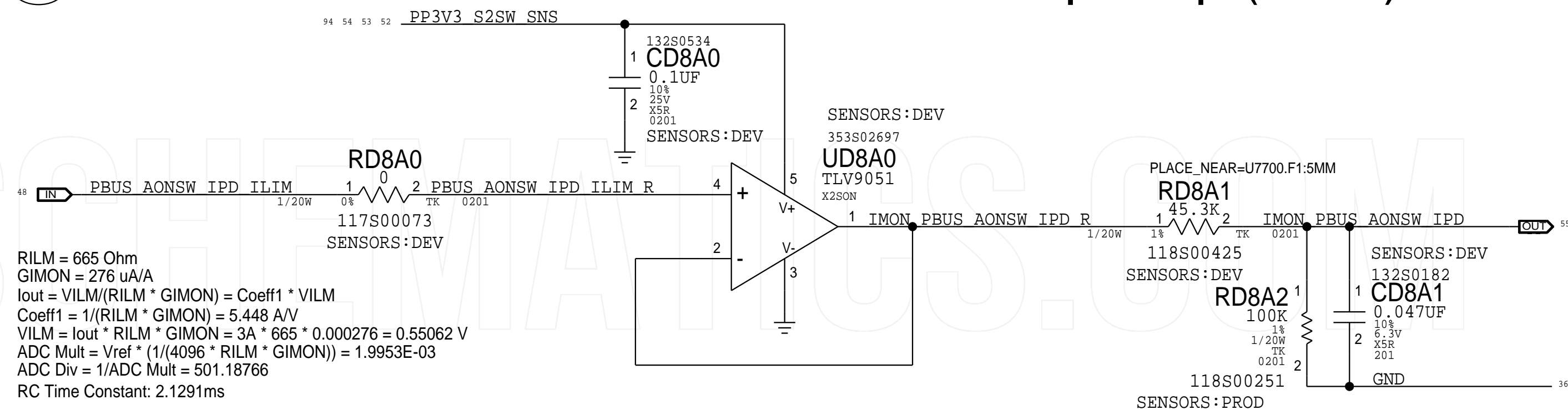
C PP3V3_S2SW_IPD Current Sense Op-Amp (IT3C)

RILM = 4.42kOhm
GIMON = 276 uA/A
Iout = VILM/(RILM * GIMON) = Coeff1 * VILM
Coeff1 = 1/(RILM * GIMON) = 0.81972588 A/V
VILM = Iout * RILM * GIMON = 0.1A * 4420 * 0.000276 = 0.12199 V
ADC Mult = Vref * (1/(4096 * RILM * GIMON)) = 3.00193E-04
ADC Div = 1/ADC Mult = 3331.1949
RC Time Constant: 2.1291ms



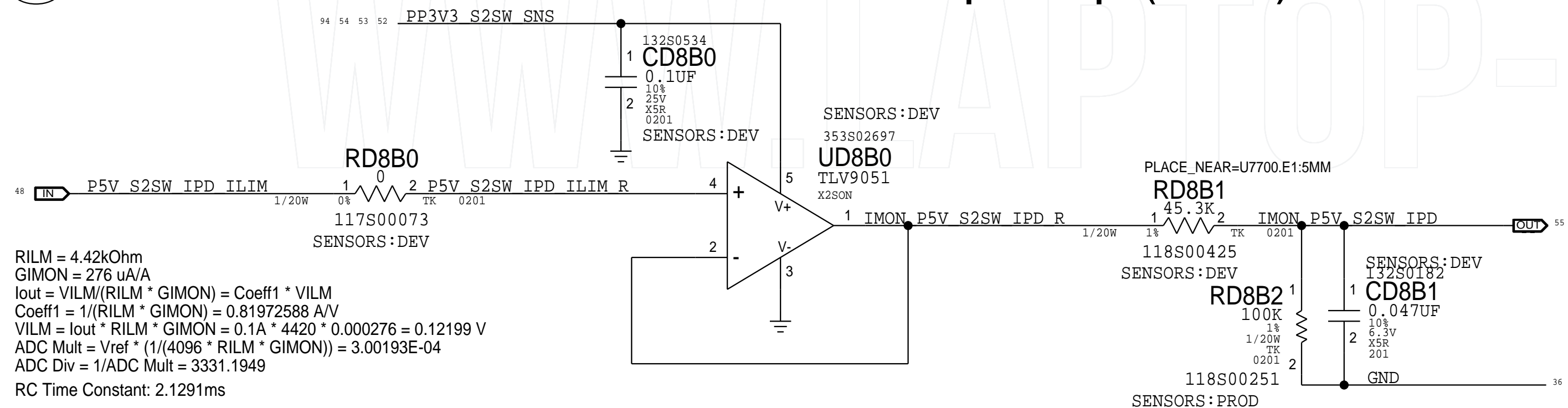
G PPBUS_AONSW_IPD Current Sense Op-Amp (ITPR)

RILM = 665 Ohm
GIMON = 276 uA/A
Iout = VILM/(RILM * GIMON) = Coeff1 * VILM
Coeff1 = 1/(RILM * GIMON) = 5.448 A/V
VILM = Iout * RILM * GIMON = 3A * 665 * 0.000276 = 0.55062 V
ADC Mult = Vref * (1/(4096 * RILM * GIMON)) = 1.9953E-03
ADC Div = 1/ADC Mult = 501.18766
RC Time Constant: 2.1291ms



D PP5V_S2SW_IPD Current Sense Op-Amp (IT5C)

RILM = 4.42kOhm
GIMON = 276 uA/A
Iout = VILM/(RILM * GIMON) = Coeff1 * VILM
Coeff1 = 1/(RILM * GIMON) = 0.81972588 A/V
VILM = Iout * RILM * GIMON = 0.1A * 4420 * 0.000276 = 0.12199 V
ADC Mult = Vref * (1/(4096 * RILM * GIMON)) = 3.00193E-04
ADC Div = 1/ADC Mult = 3331.1949
RC Time Constant: 2.1291ms



H Production Sensor BOM Table

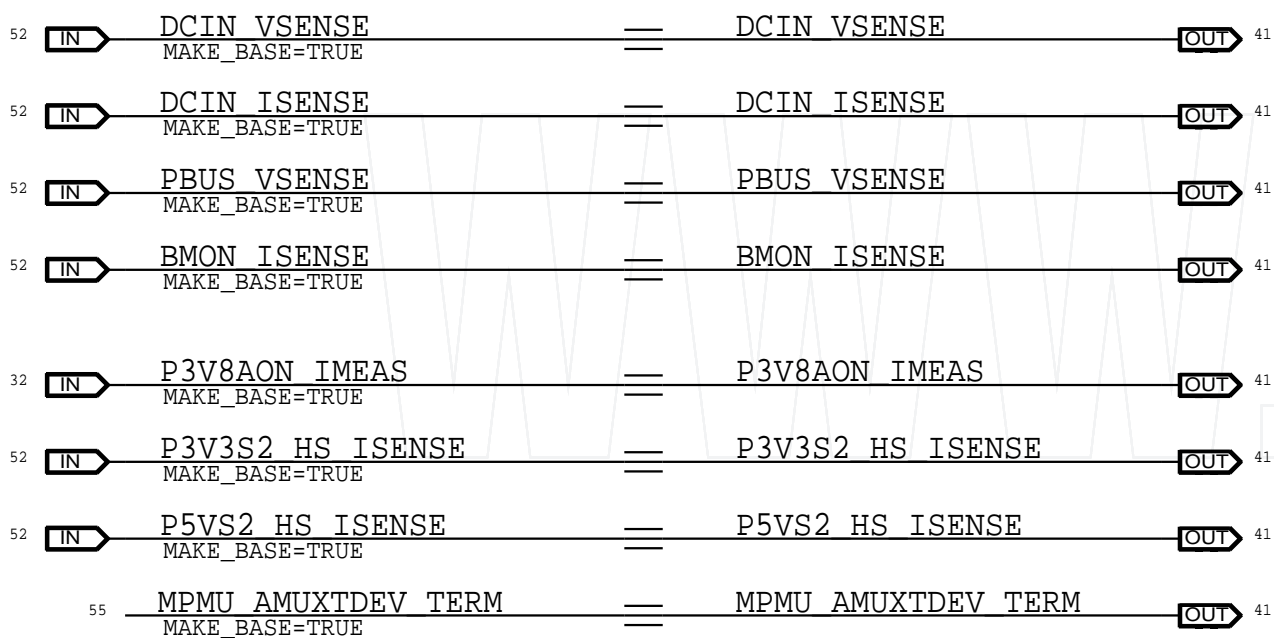
PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
117S00095	1	RES,TK,100K OHM,5%,1/20W,0201	RD819		SENSORS:PROD
117S00095	1	RES,TK,100K OHM,5%,1/20W,0201	RD889		SENSORS:PROD

SENSORS: POWER LOW SIDE (1/2)		
	DRAWING NUMBER	051-07020
	REVISION	6.0.0
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	PAGE	138 OF 801
	SHEET	54 OF 113

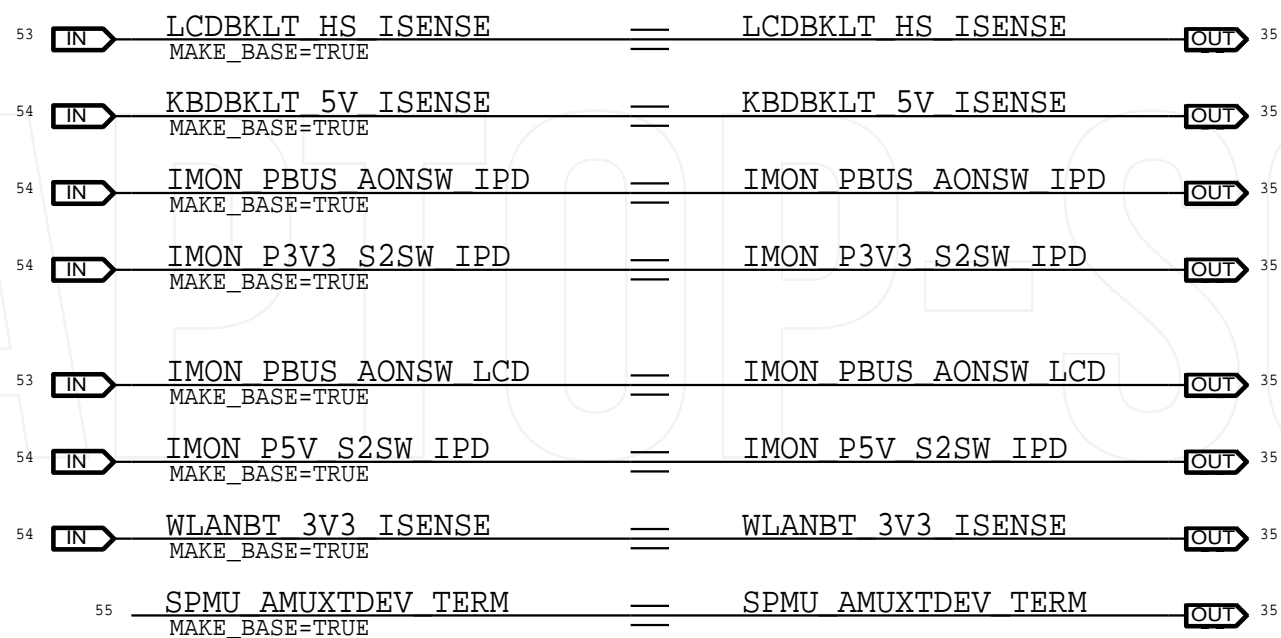
BOM_COST_GROUP=SENSORS

A ADC Input Aliases

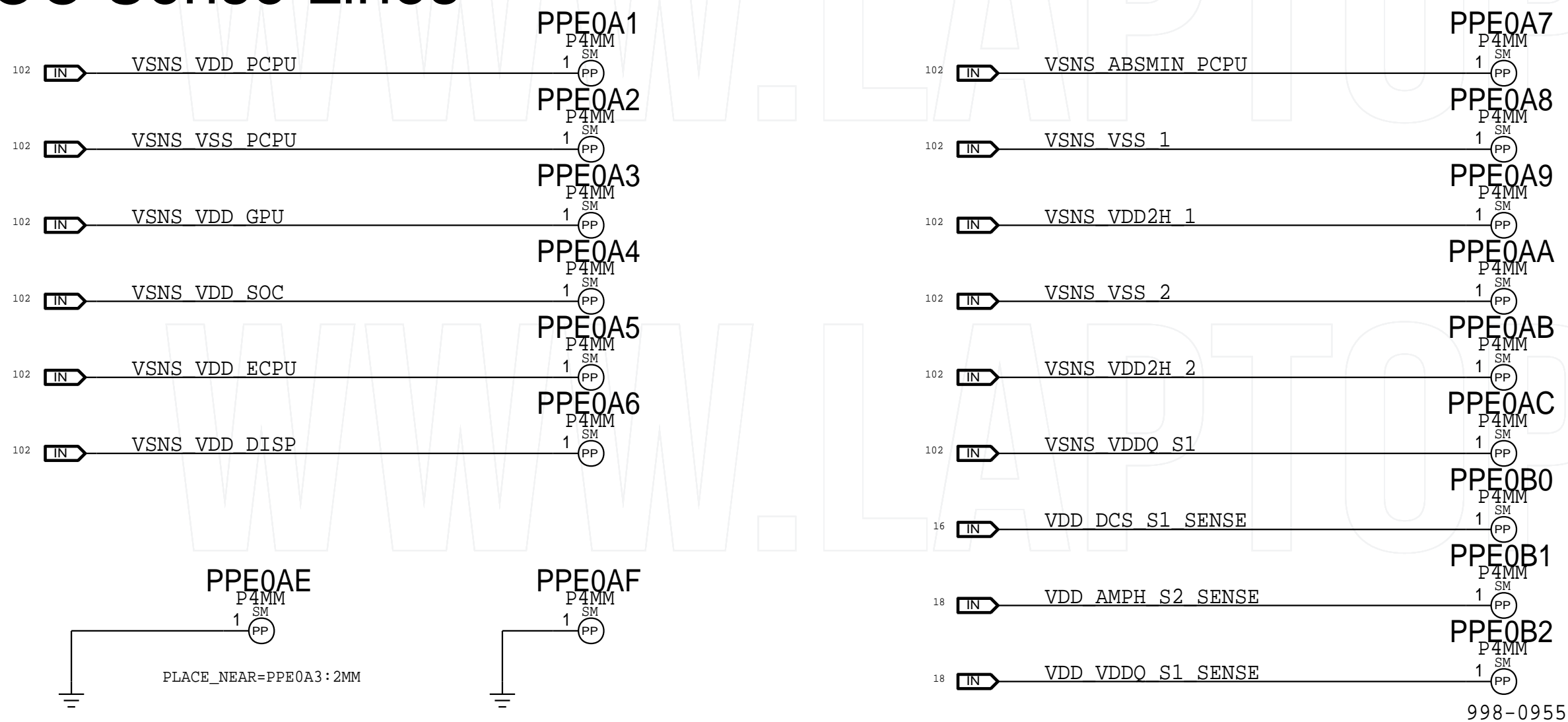
MASTER PMU AMUX ALIAS



SLAVE PMU AMUX ALIAS

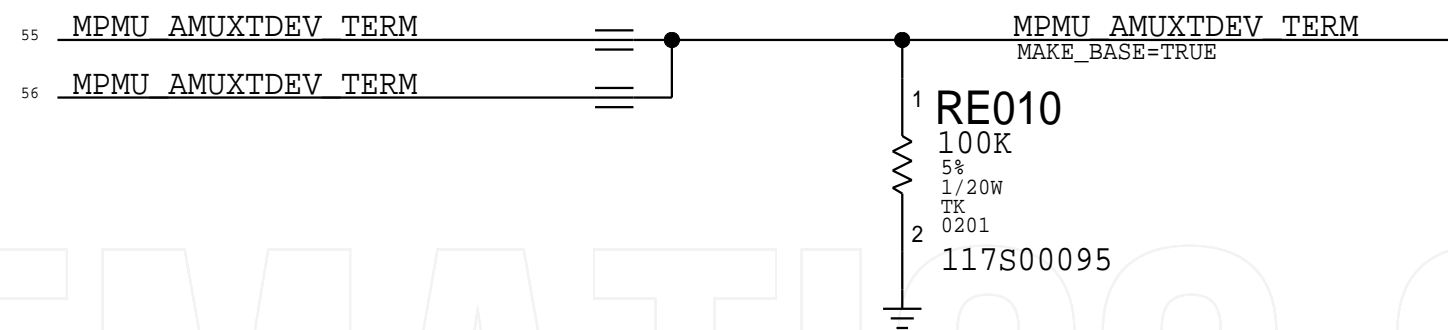


B SOC Sense Lines



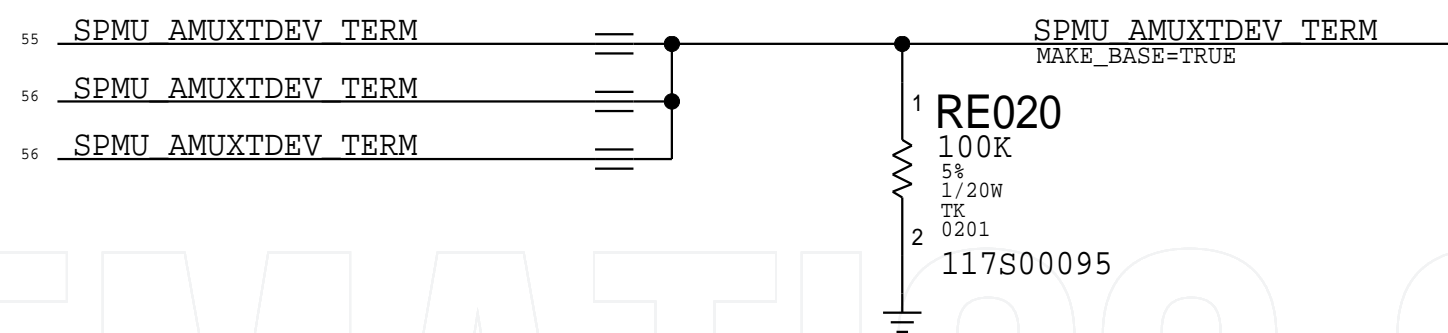
C Unused MPMU AMUX/TDEV Termination

RECOMMENDED NOT TO LEAVE AMUX/TDEV FLOATING.



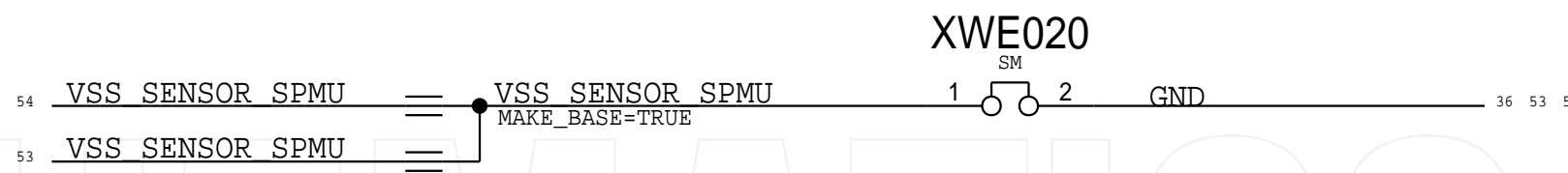
D Unused SPMU AMUX/TDEV Termination

RECOMMENDED NOT TO LEAVE AMUX/TDEV FLOATING.



E I/V Sensor Ground Reference Aliases

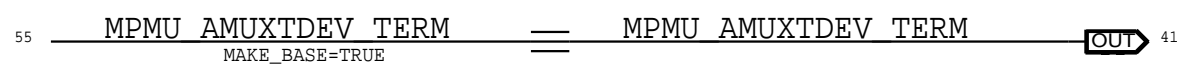
Slave PMU ADC Ground Alias



PAGE TITLE		
SENSORS: POWER SUPPORT		
	DRAWING NUMBER	051-07020
	REVISION	6.0.0
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	PAGE	140 OF 801
	SHEET	55 OF 113

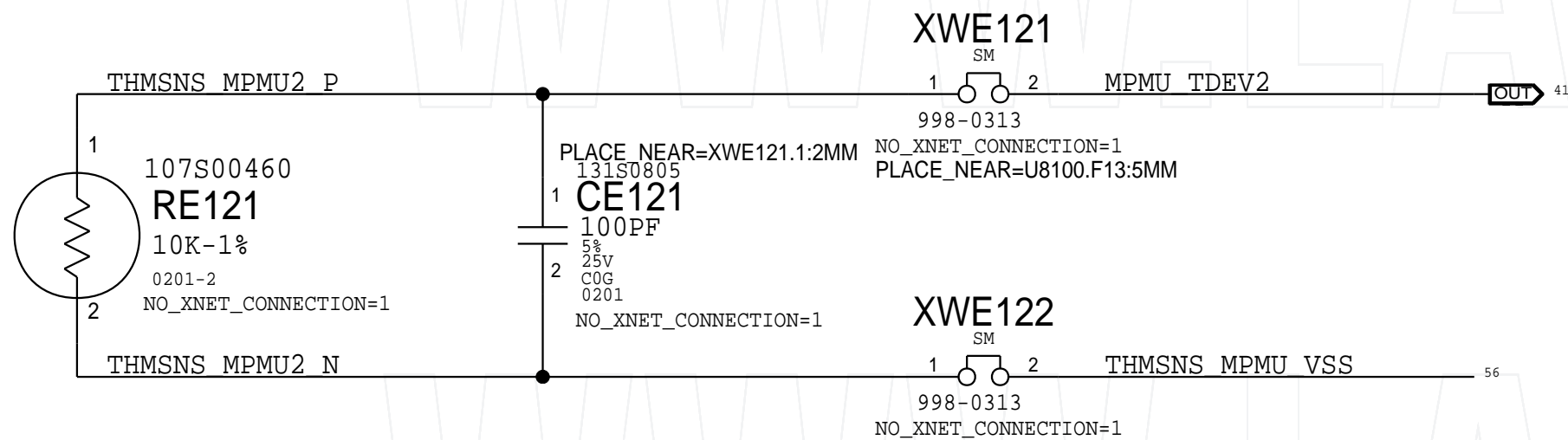
A Master PMU TDEV1 (Txxx)

Location: TBD



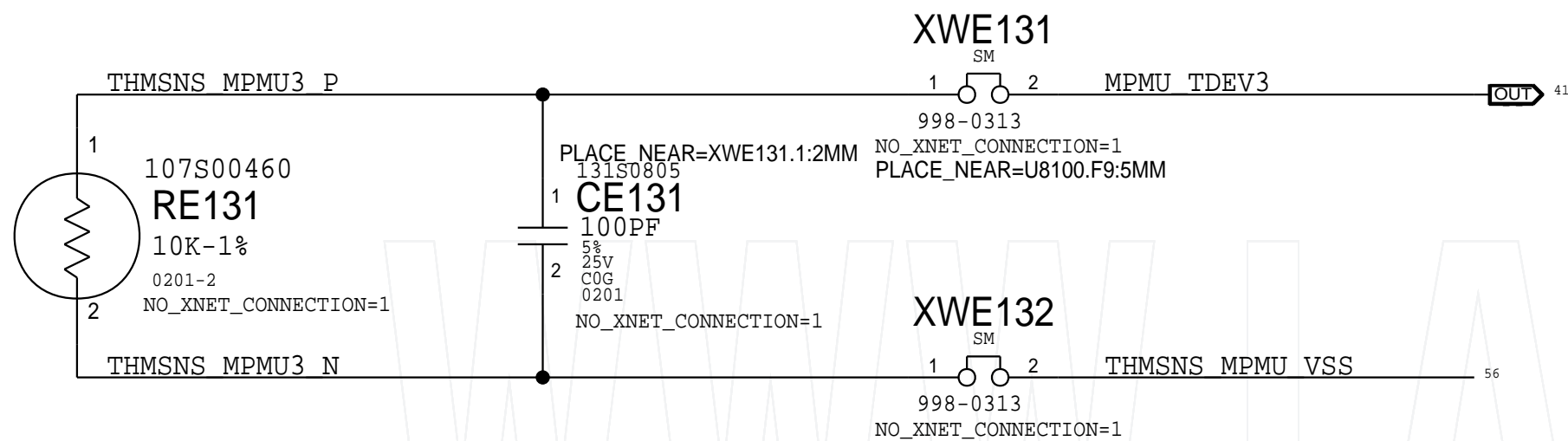
B Master PMU TDEV2 (Tm0B)

Location: Ambient



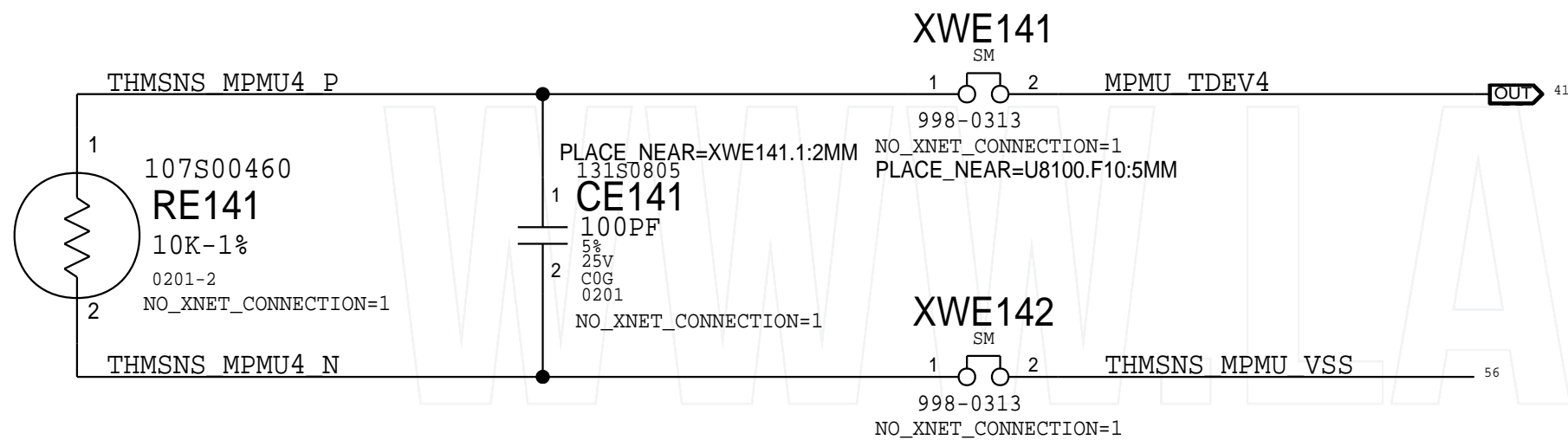
C Master PMU TDEV3 (TIOP)

Location: Thunderbolt Proximity

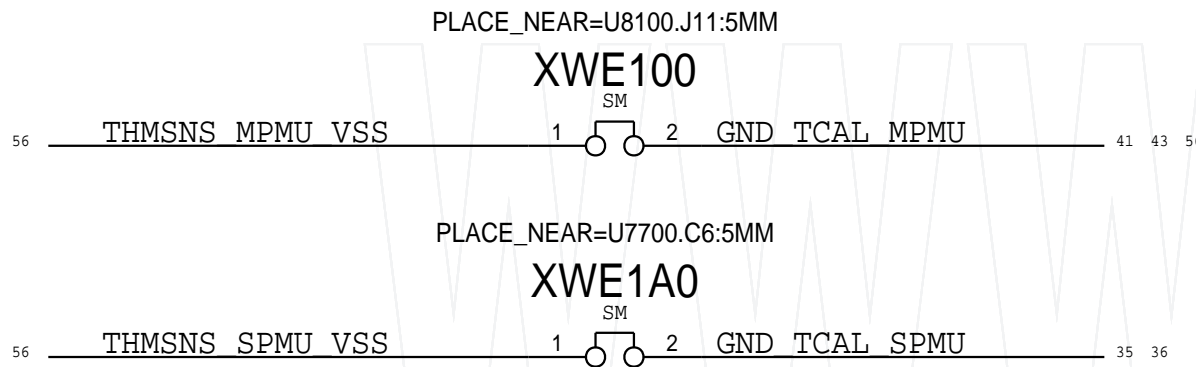


D Master PMU TDEV4 (TW0P)

Location: Wireless Proximity

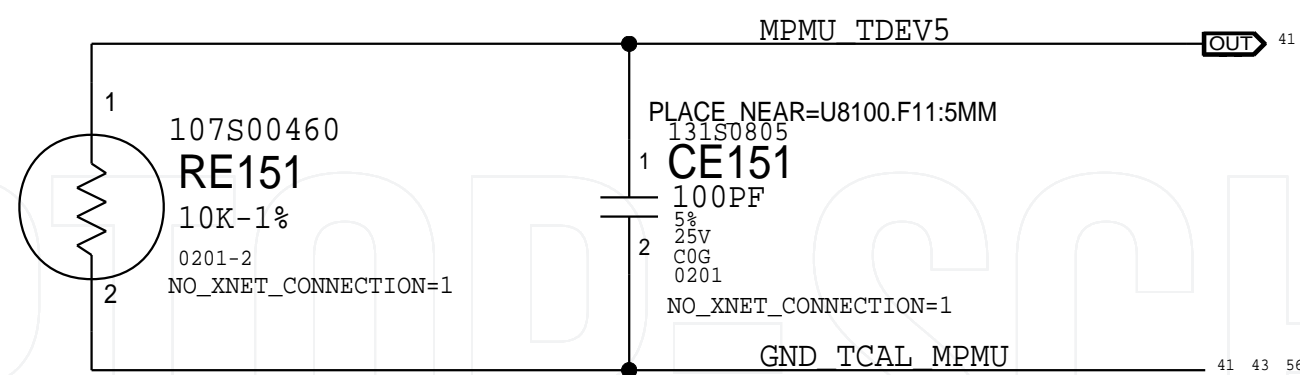


E Master/Slave PMU VSS Connection



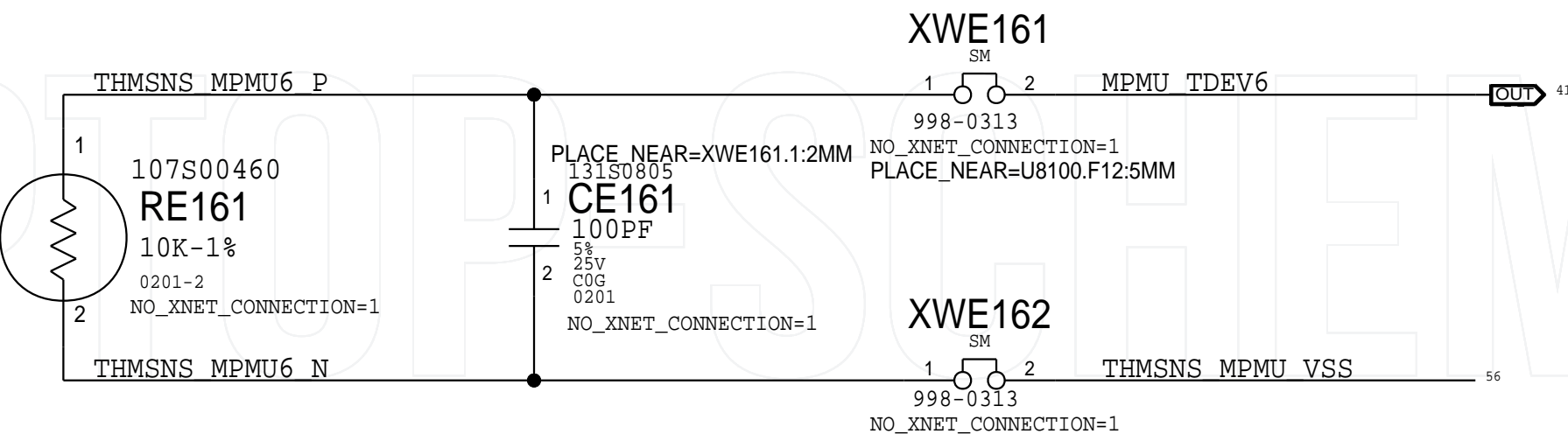
F Master PMU TDEV5 (TPMP)

Location: Master PMU Proximity



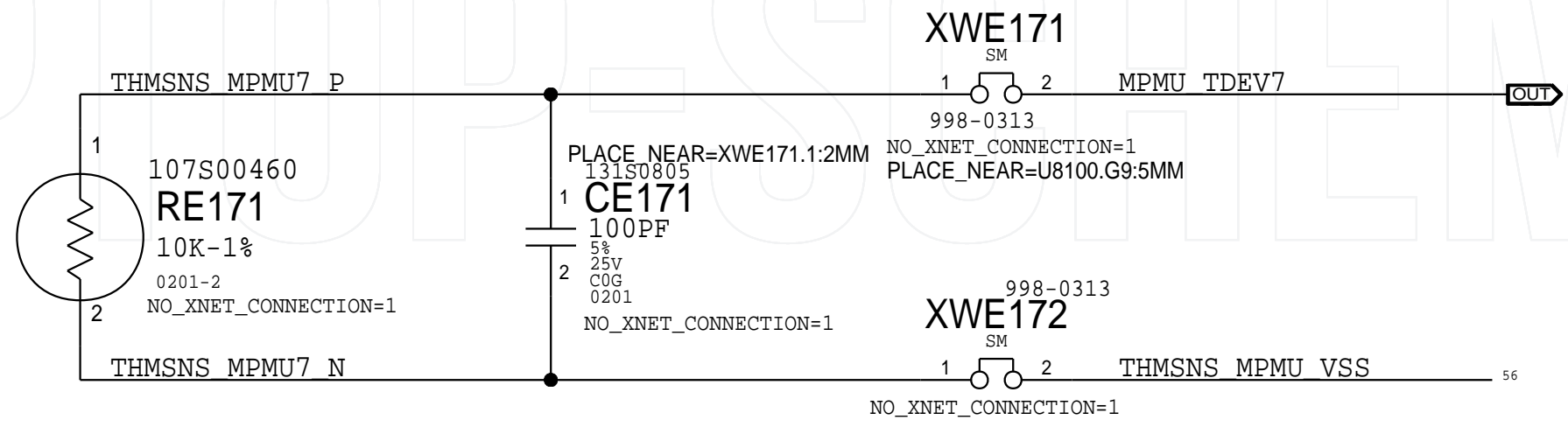
G Master PMU TDEV6 (T5SP)

Location: PP5V_S2 (UC300)



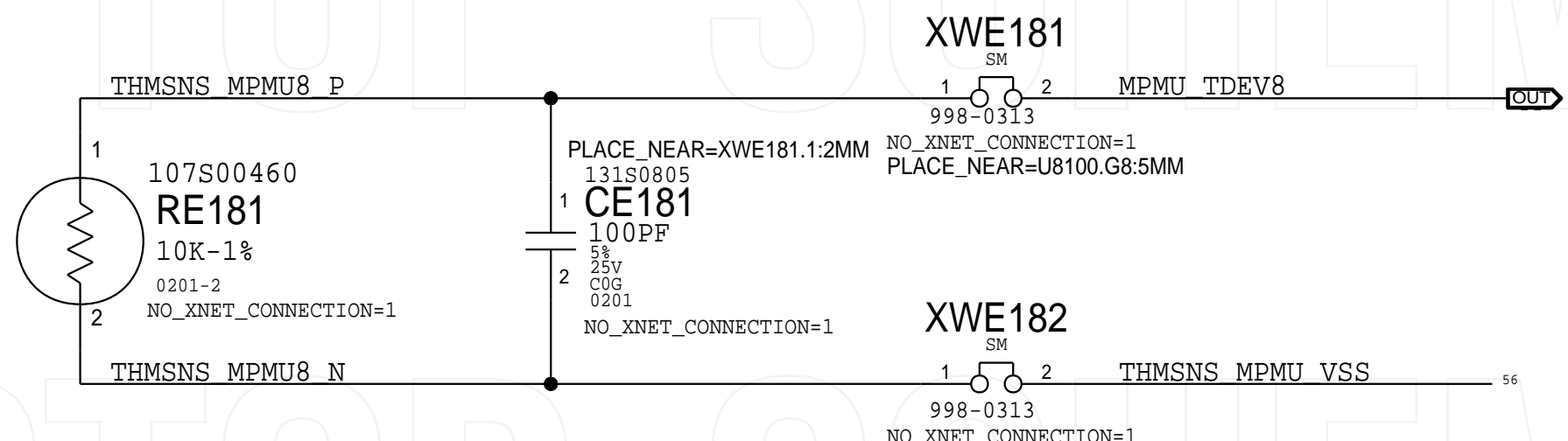
H Master PMU TDEV7 (TCHP)

Location: Charger Proximity



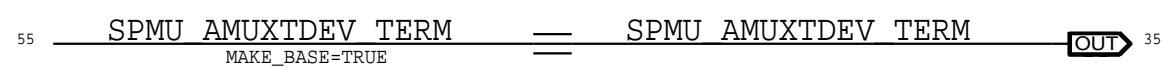
I Master PMU TDEV8 (TMVR)

Location: Main VR (PP3V8_AON_VDDMAIN)



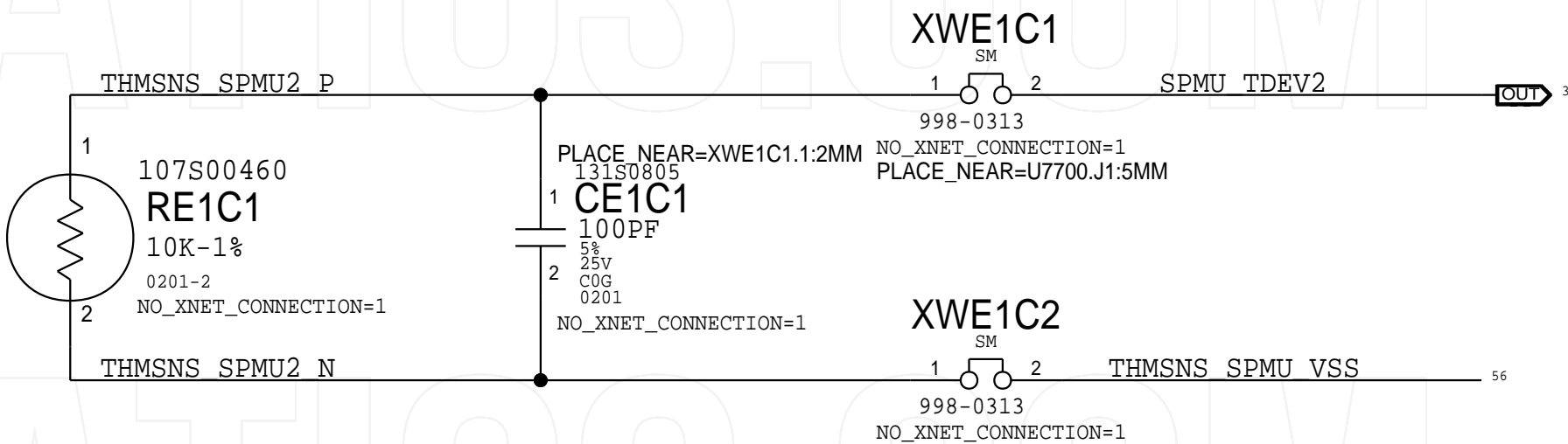
J Slave PMU TDEV1 (Txxx)

Location: TBD



K Slave PMU TDEV2 (TH0T)

Location: NAND Proximity



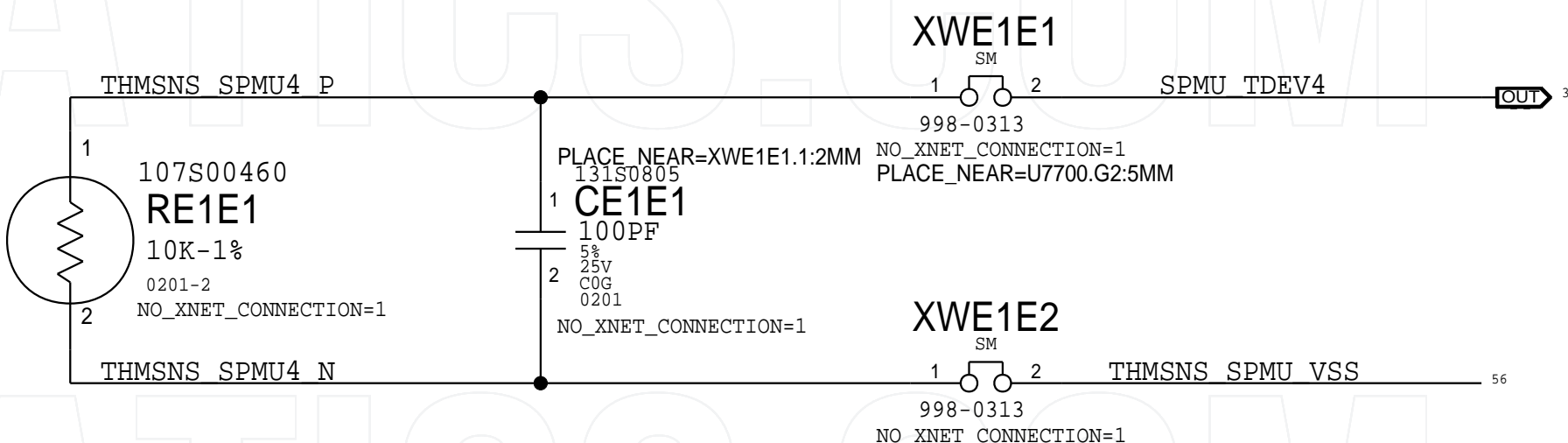
L Slave PMU TDEV3 (Txxx)

Location: TBD



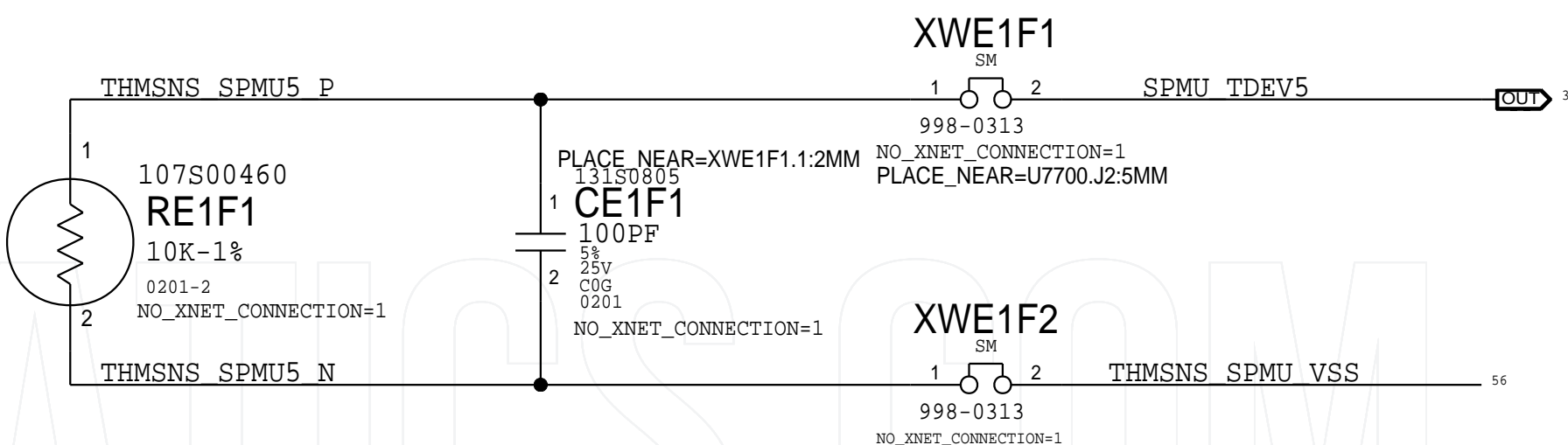
M Slave PMU TDEV4 (TSCD)

Location: SOC Proximity



N Slave PMU TDEV5 (TPSP)

Location: Slave PMU Proximity

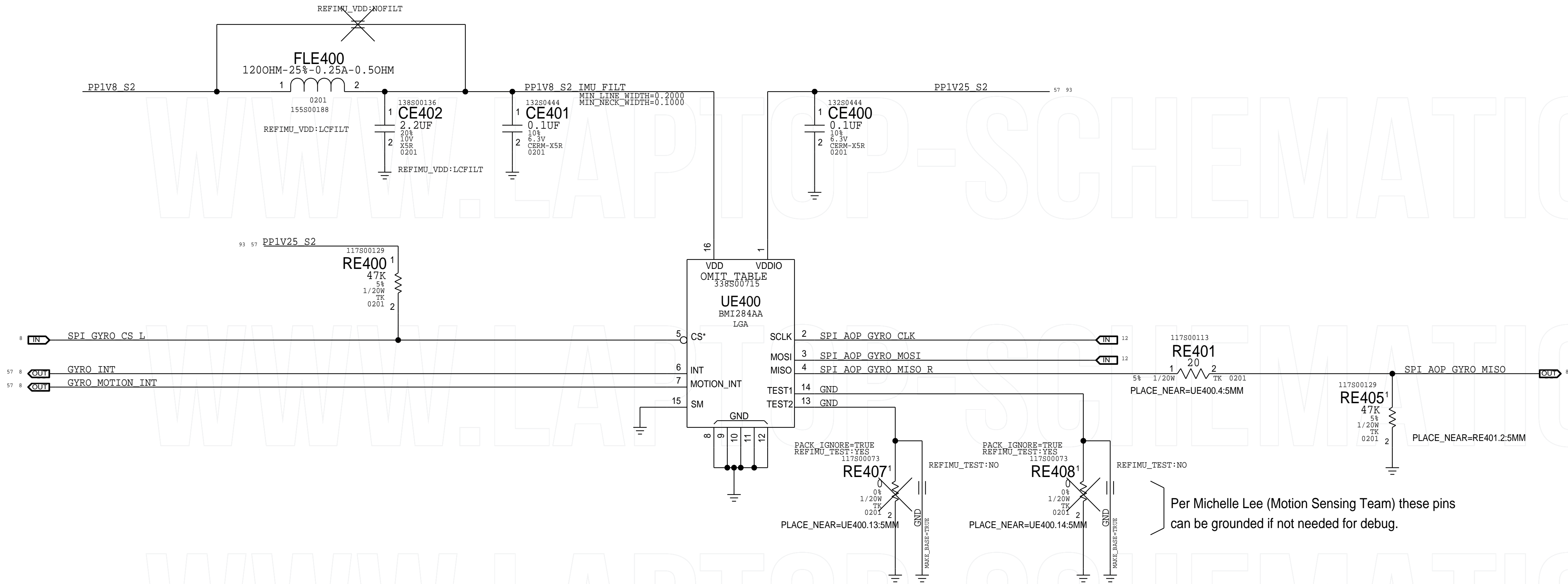


PAGE TITLE			SENSORS: THERMAL		
			DRAWING NUMBER	051-07020	SIZE
			REVISION	6.0.0	D
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			PAGE	141 OF 801	
			SHEET	56 OF 113	

BOM_COST_GROUP=SENSORS

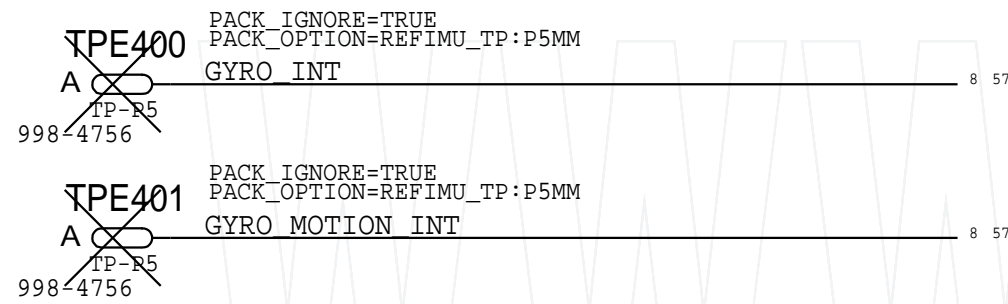
A Sovereign Accelerometer and Gyroscope

*** OK2INTEGRATE ***



MFG: Bosch
MPN: BMI284AA
APN: 338S00715
URL: <https://www.bosch-sensortec.com/products/motion-sensors/imus/>
Radar: [rdar://61521702](https://www.bosch-sensortec.com/products/motion-sensors/imus/) (Sovereign: Datasheet)

B Test Points



C Sovereign BOM Options

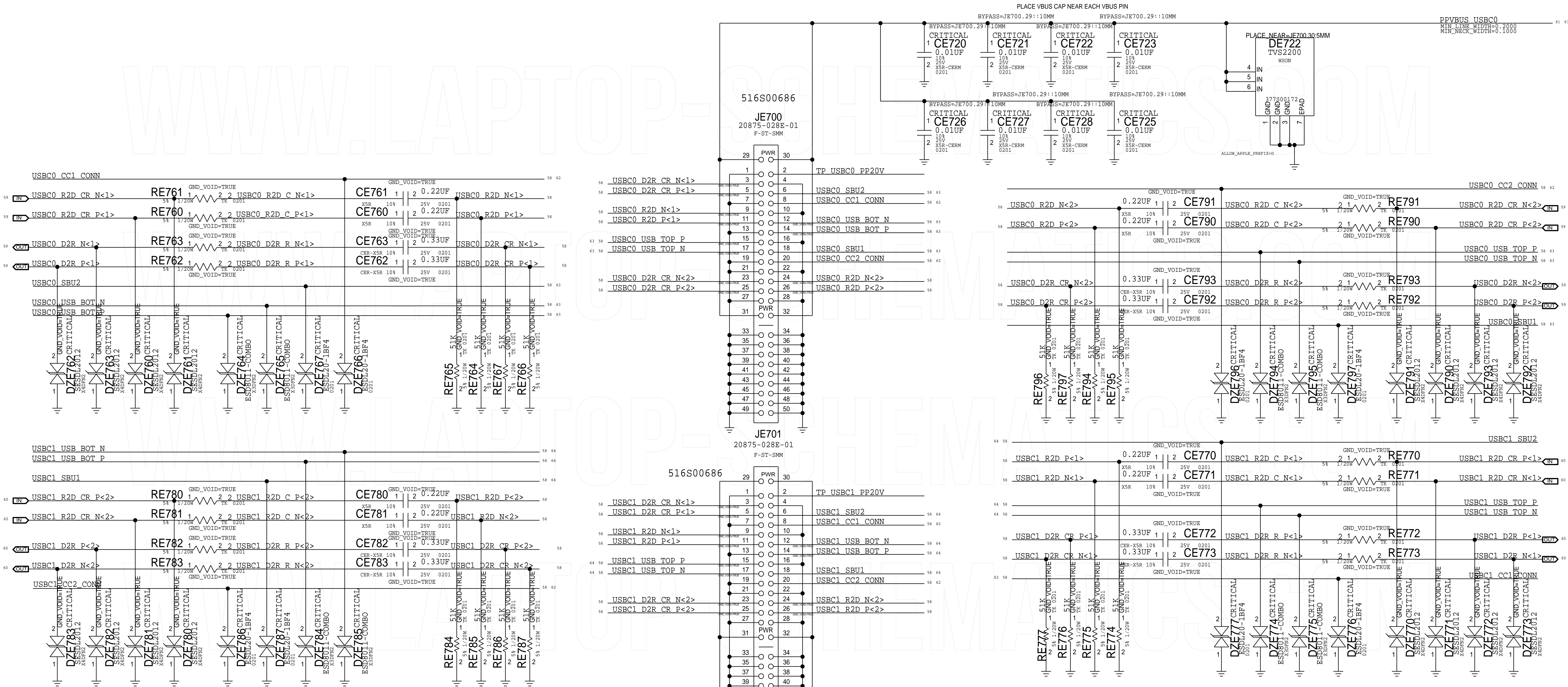
PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
338S00715	1	IC, SOVEREIGN, BMI284, AA, LGA16	UE400	CRITICAL	REFIMU_IC: BMI284
338S00849	1	IC, SOVEREIGN2, BMI286, AA, LGA16	UE400	CRITICAL	REFIMU_IC: BMI286

SENSORS: MOTION		
	DRAWING NUMBER	051-07020
	REVISION	6.0.0
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	PAGE	144 OF 801
	SHEET	57 OF 113

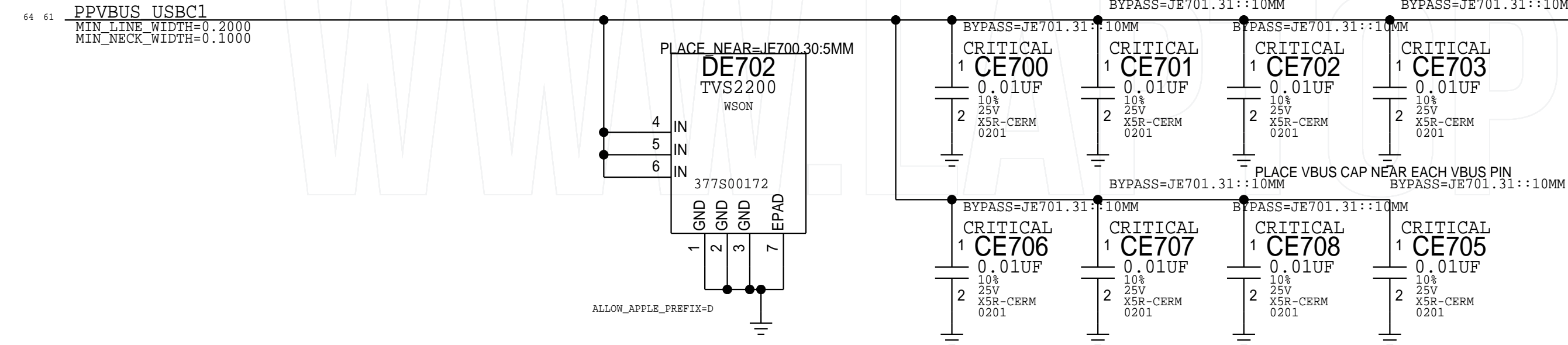
BOM_COST_GROUP=SENSORS

Left Rear Port

FOR POR, VERIFY 20% TOLERANCE ON 0.22UF AC COUPLING CAP IS OK



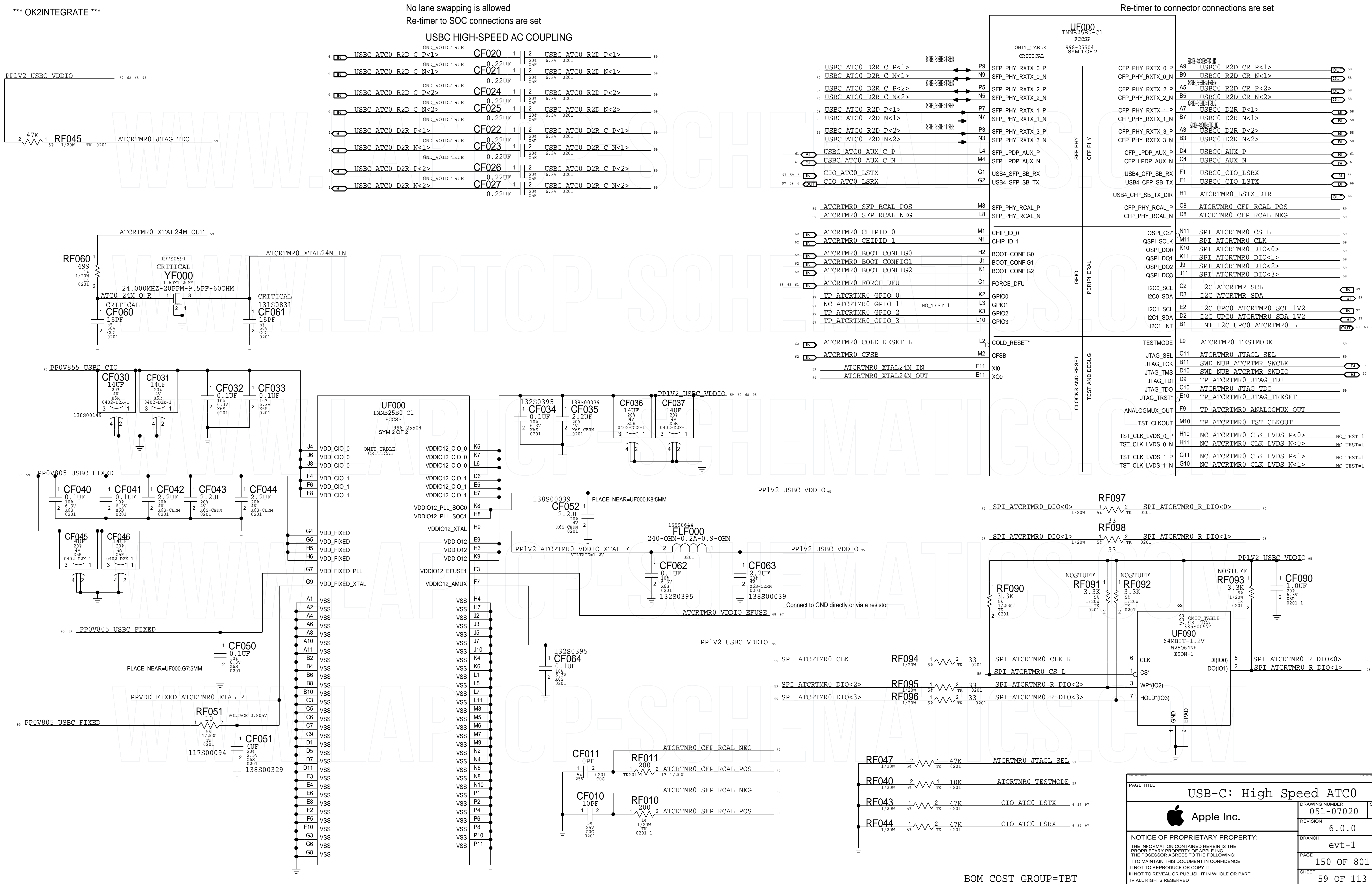
FOR POR, VERIFY 20% TOLERANCE ON 0.22UF AC COUPLING CAP IS OK

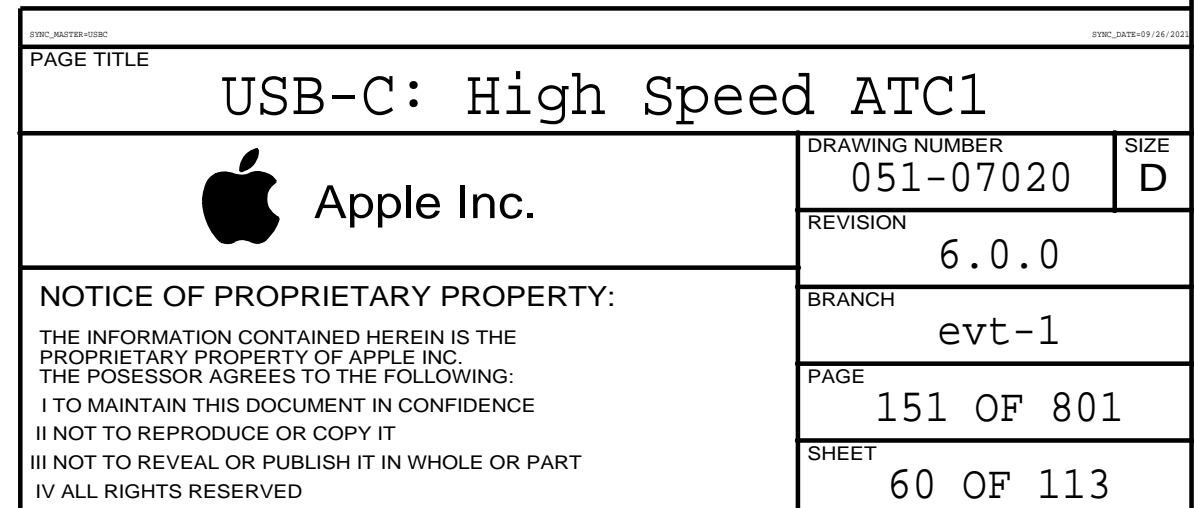


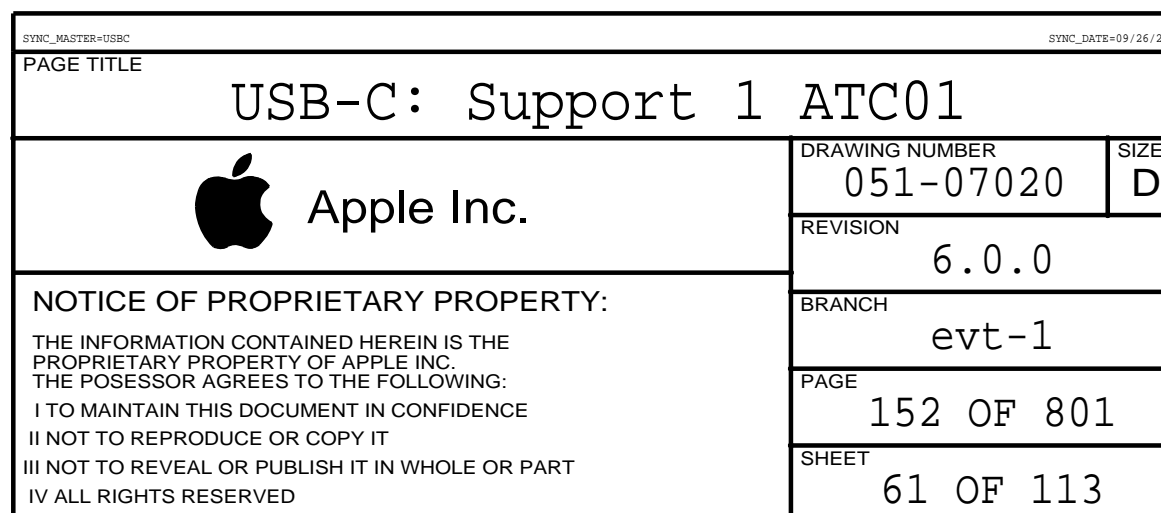
Left Front Port

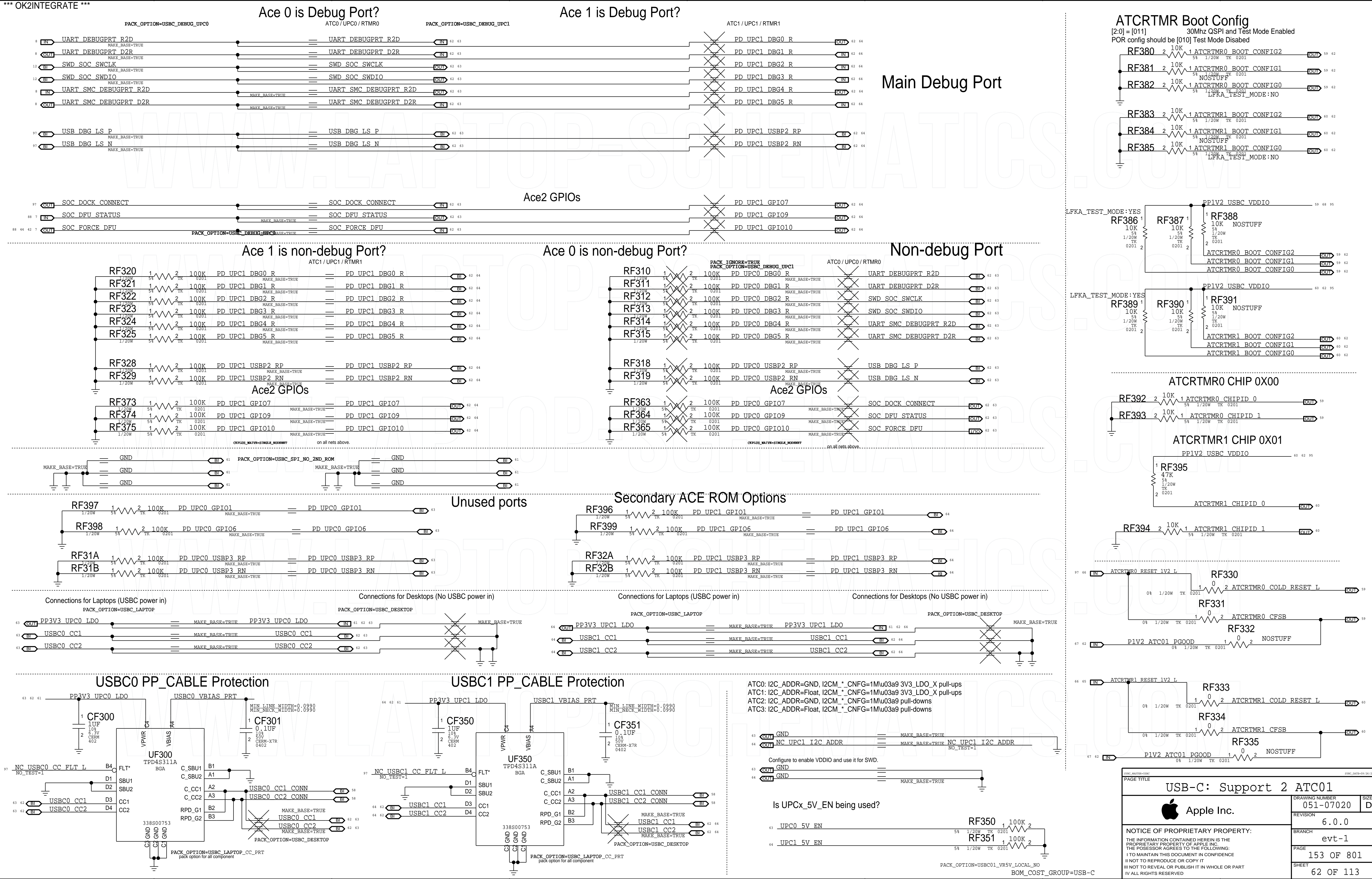
PAGE TITLE		
USB-C: Connector(s)		
	DRAWING NUMBER	051-07020
	REVISION	6.0.0
	BRANCH	evt-1
	PAGE	147 OF 801
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BOM_COST_GROUP=USB-C

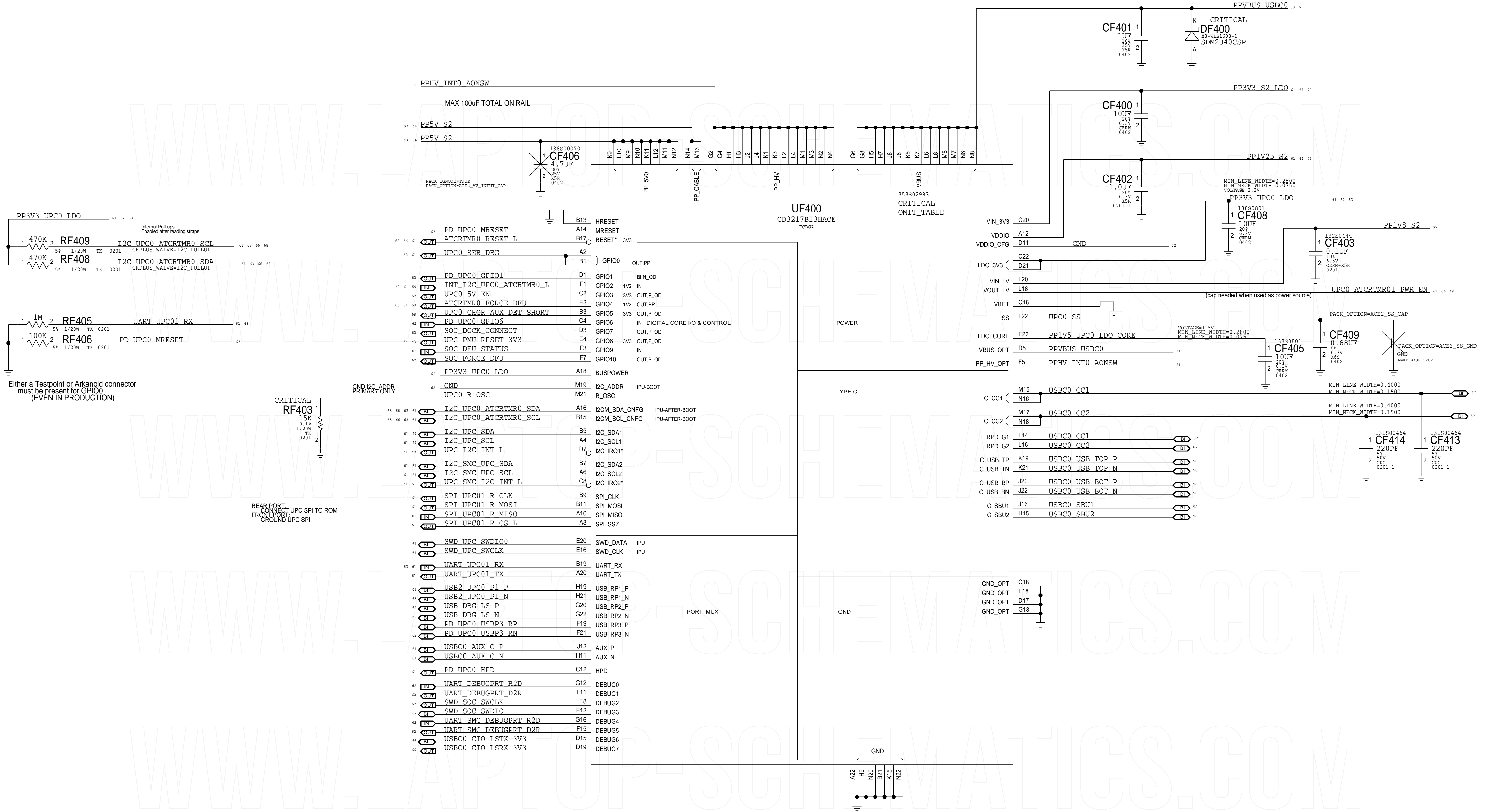






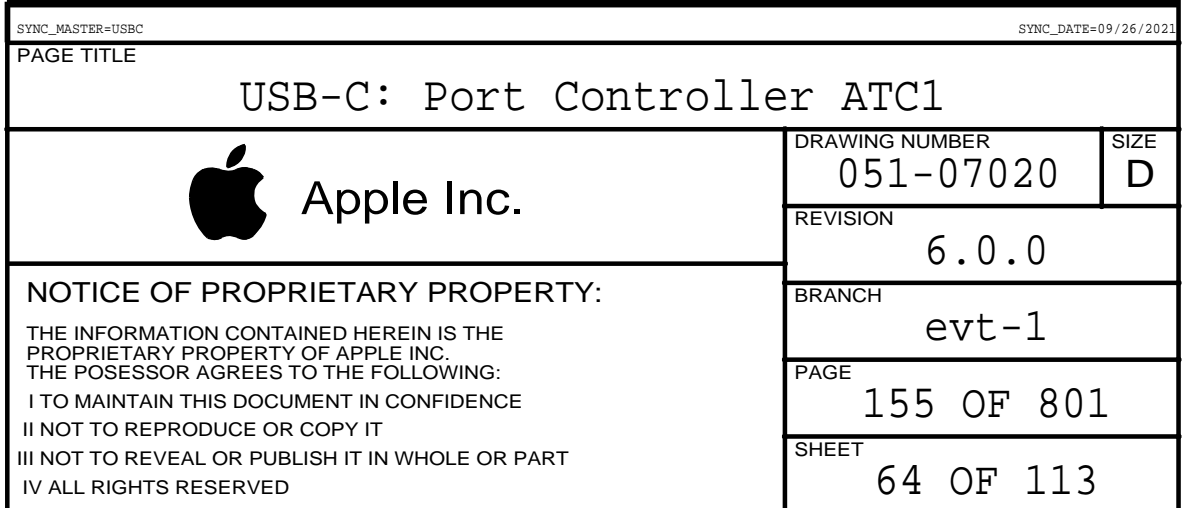


OK2INTEGRATE



PAGE TITLE			PAGE NUMBER		
USB-C: Port Controller ATC0			051-07020		
Apple Inc.			6.0.0		
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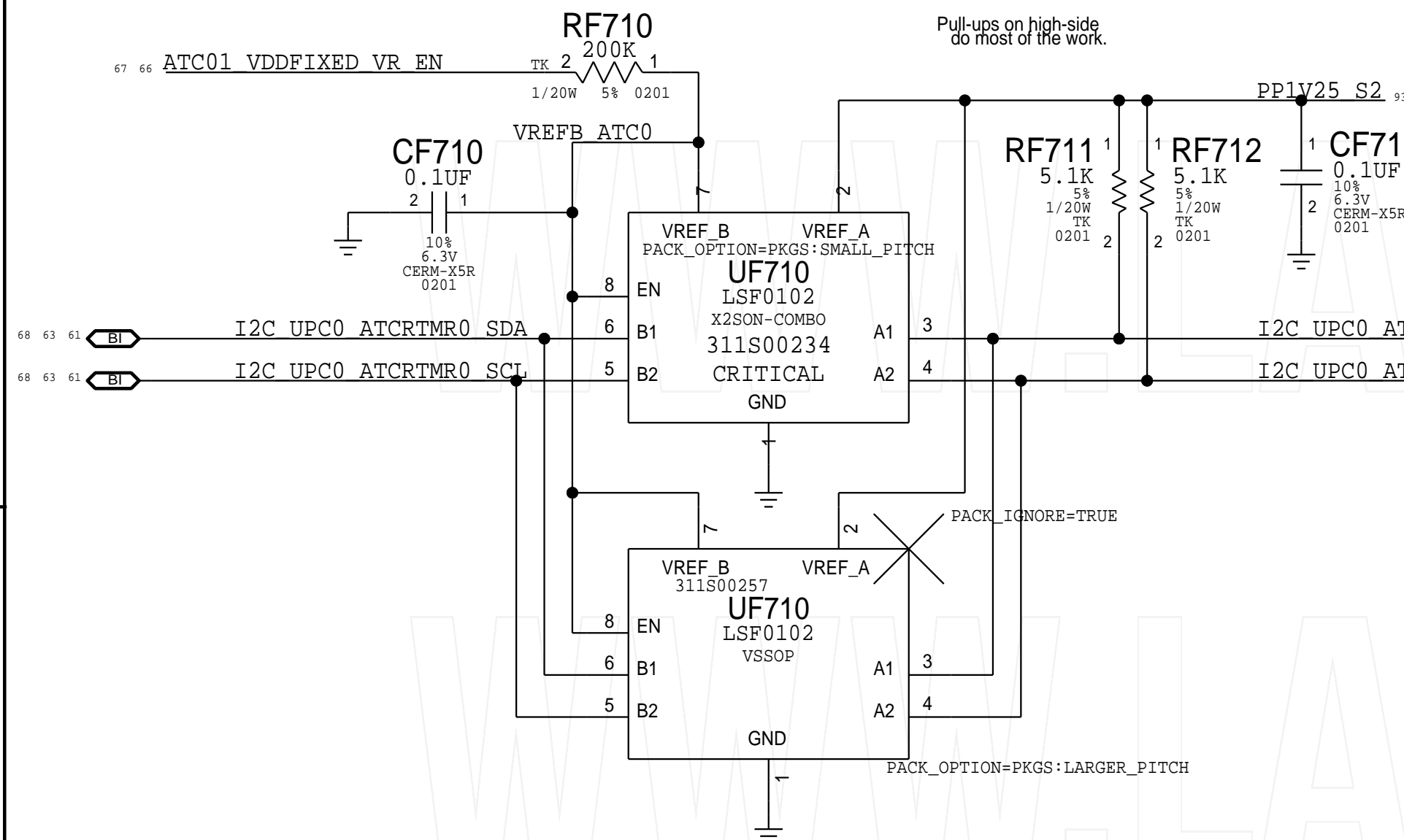
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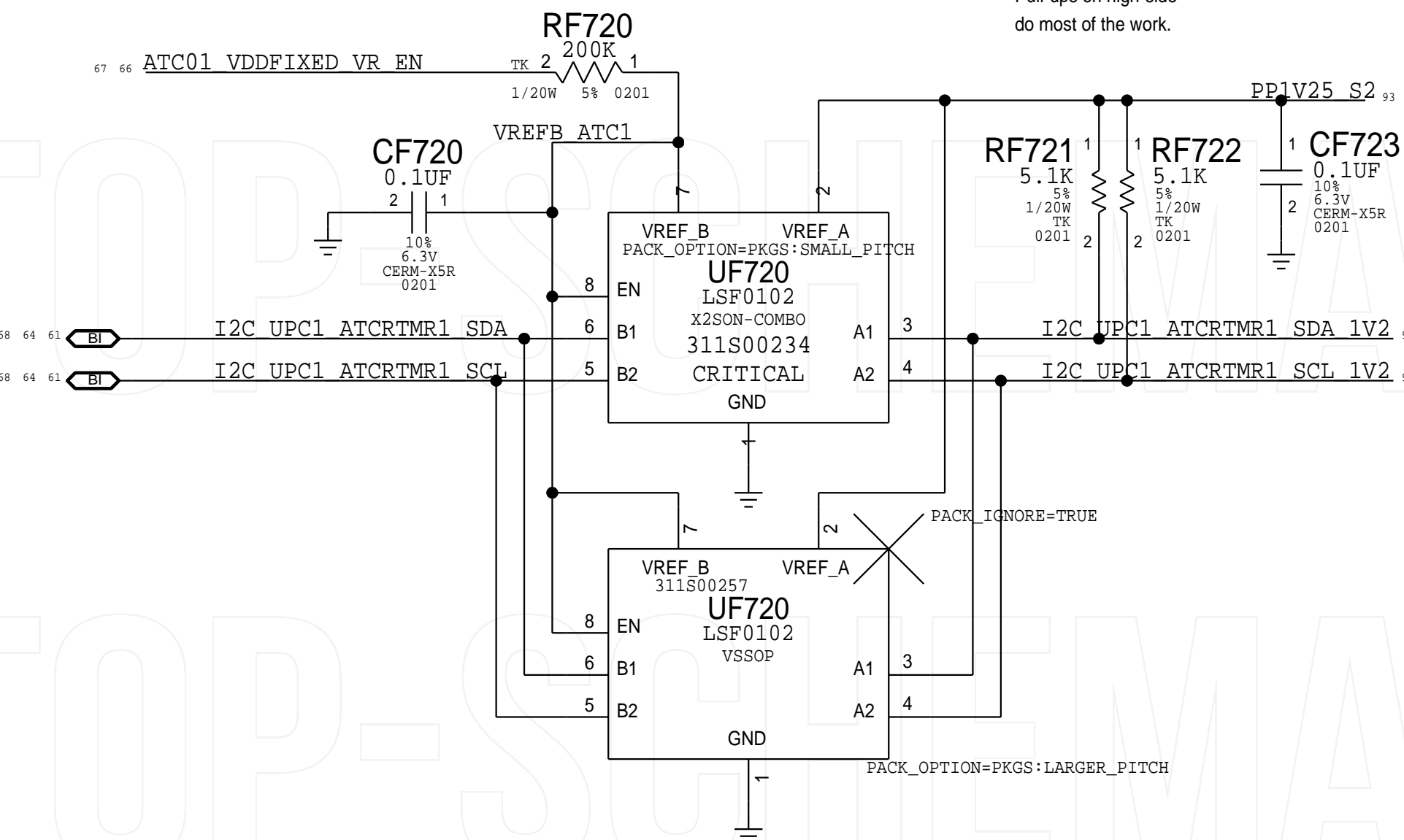
*** OK2INTEGRATE ***

Sequencing Requirements: 3.3V to UF790 --> system 1.2V (UF710,UF720) same time or before system 1.8V (UF400&UF500 VIN_LV pin)

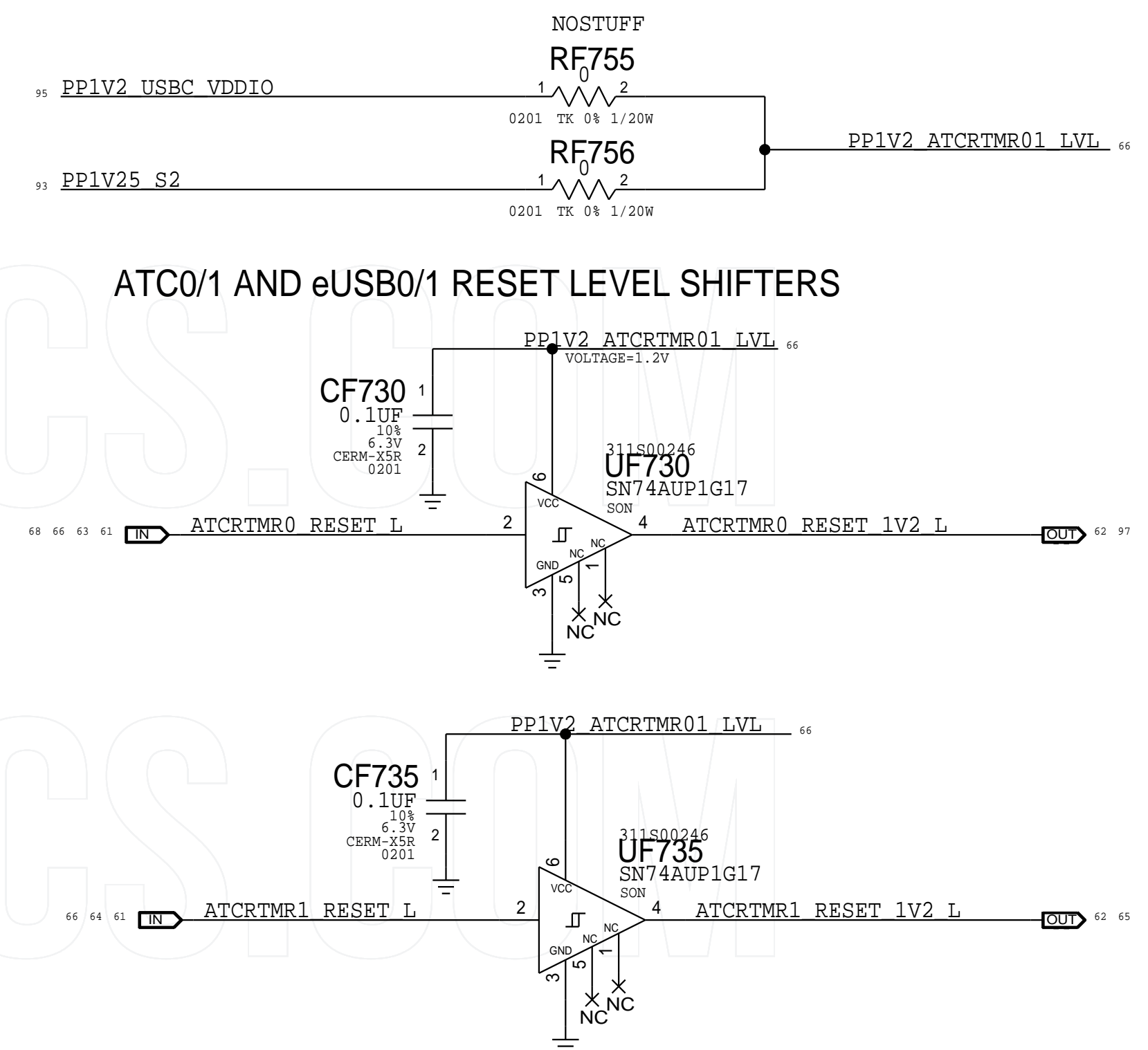
ATC0 RE-TIMER I2C LEVEL SHIFTERS



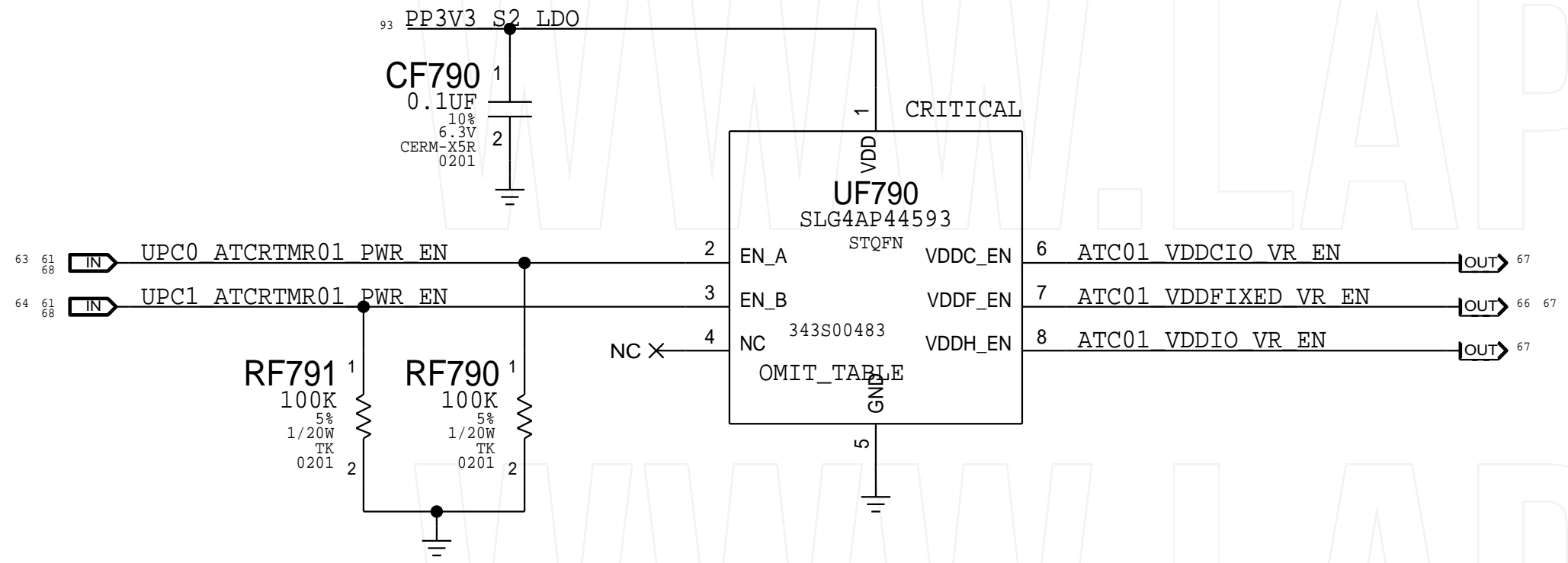
ATC1 RE-TIMER I2C LEVEL SHIFTERS



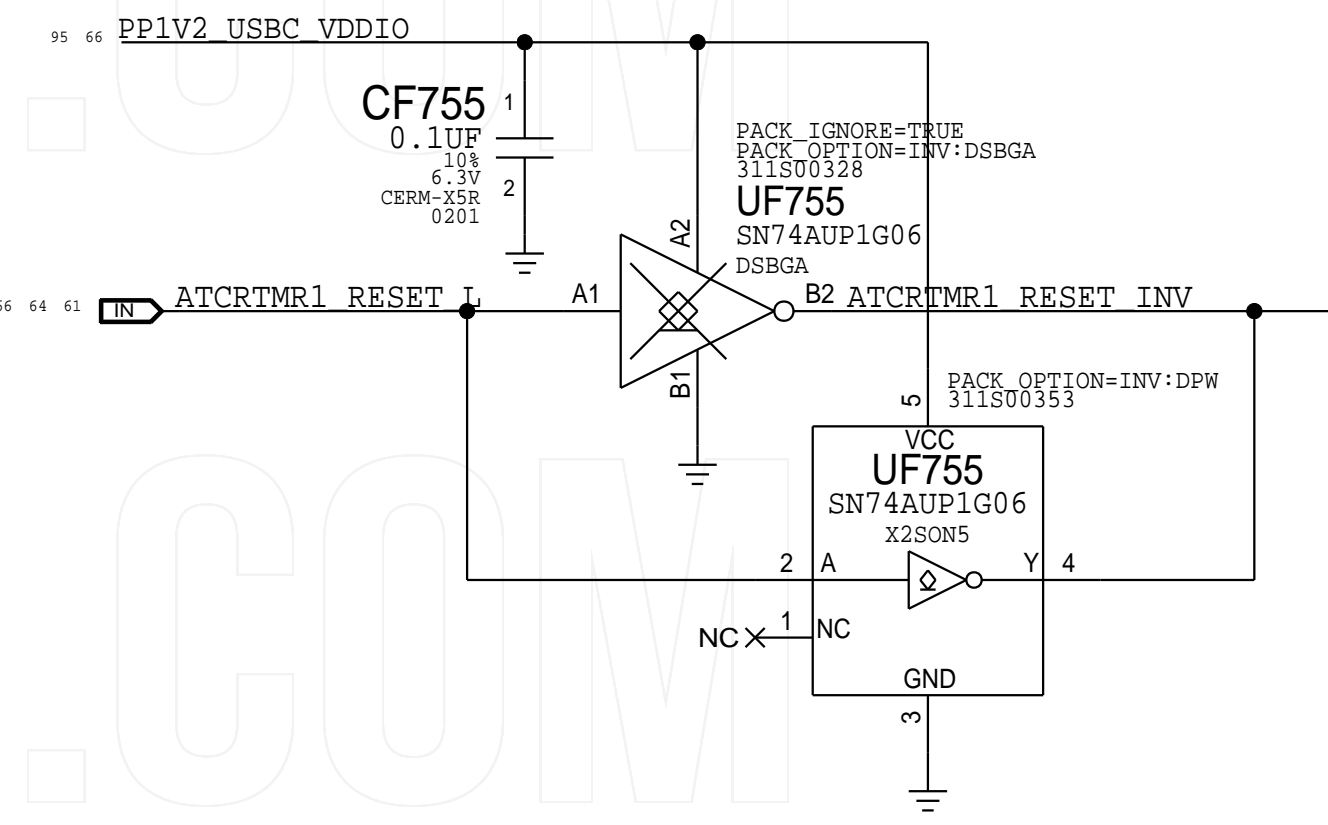
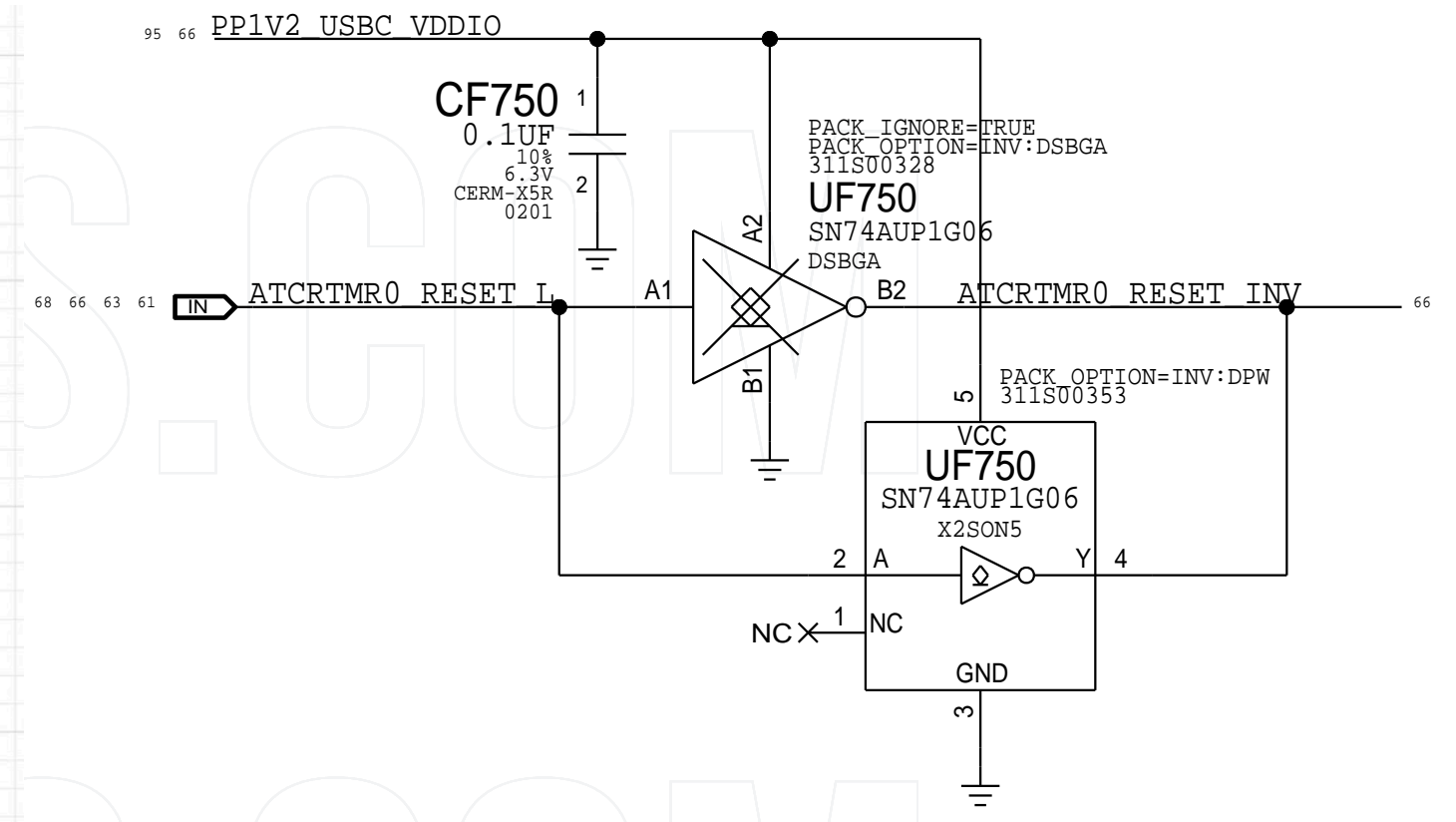
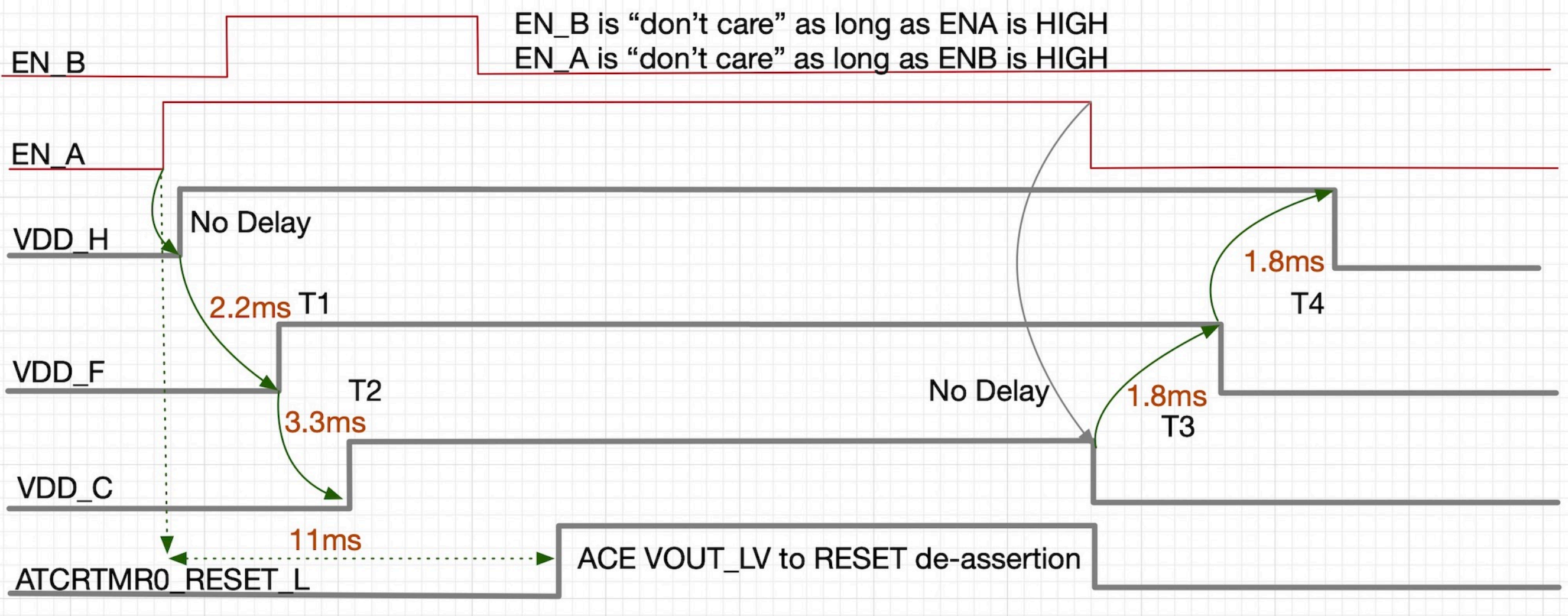
ATC0/1 AND eUSB0/1 RESET LEVEL SHIFTERS



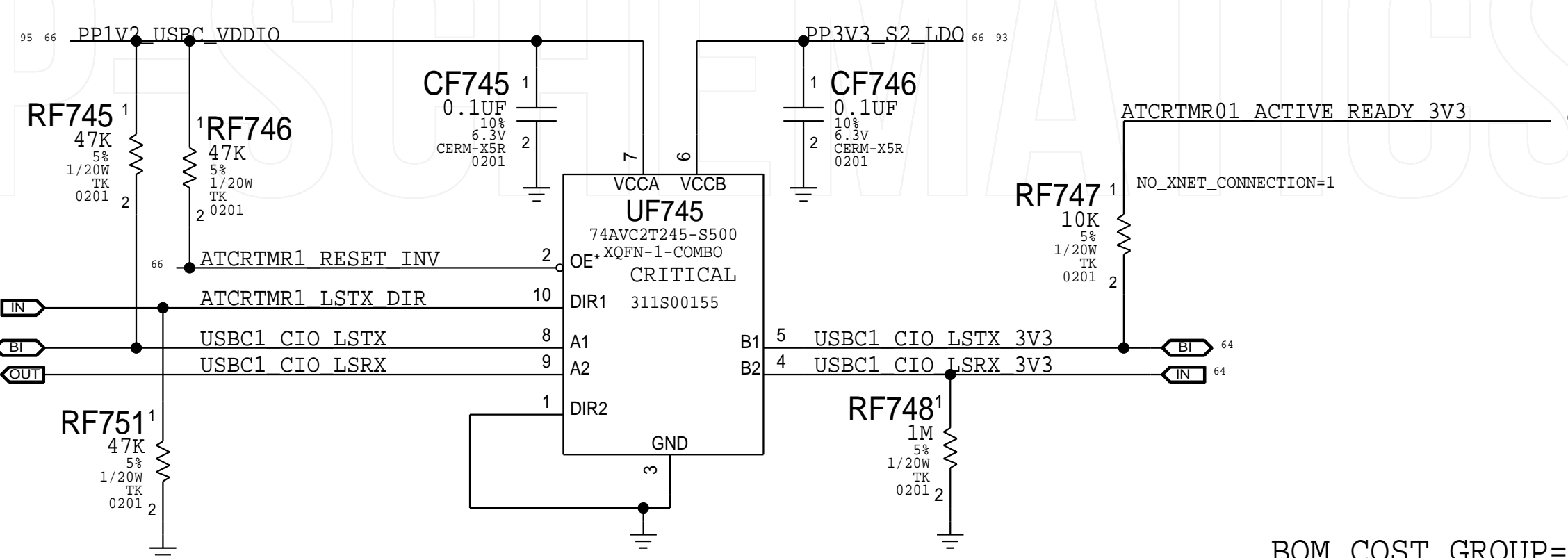
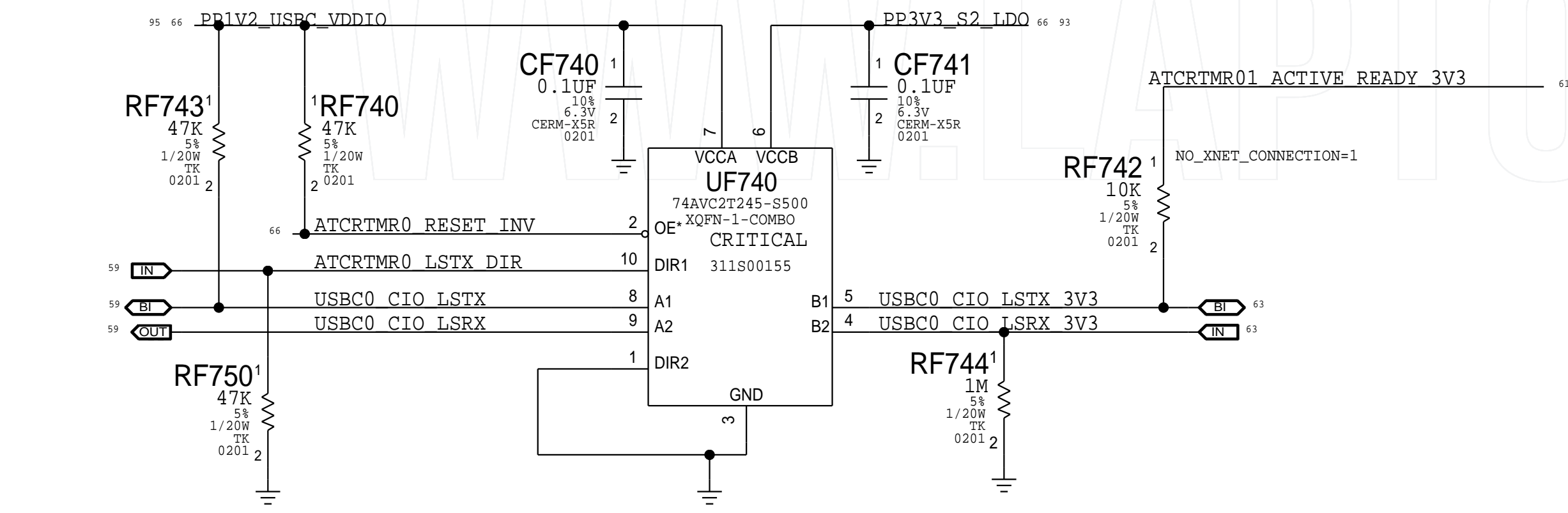
The 3.3V needs to be HIGH before VIN_LV of ACEs



Note1: As long as EN_A or EN_B are HIGH, the outputs stay HIGH
Note2: Outputs are an Ored and delayed version of EN_A or EN_B



A

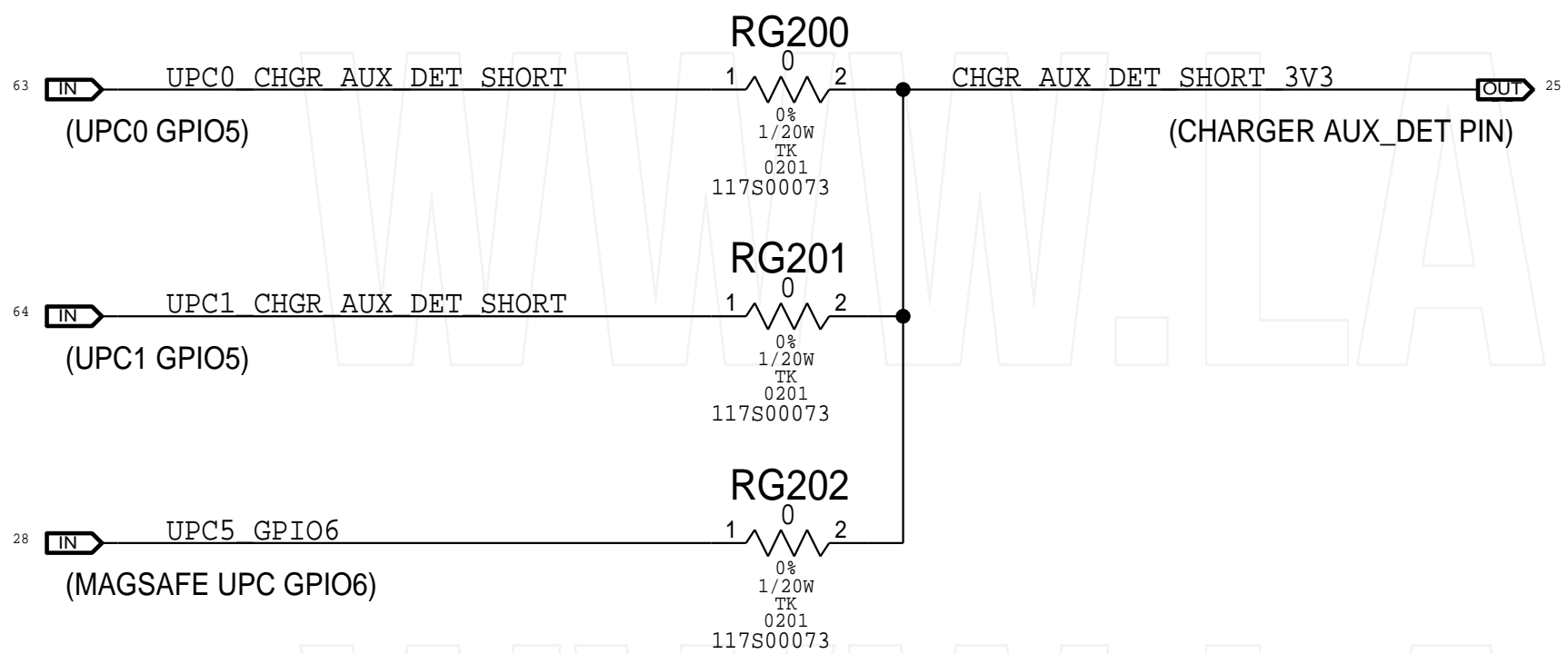


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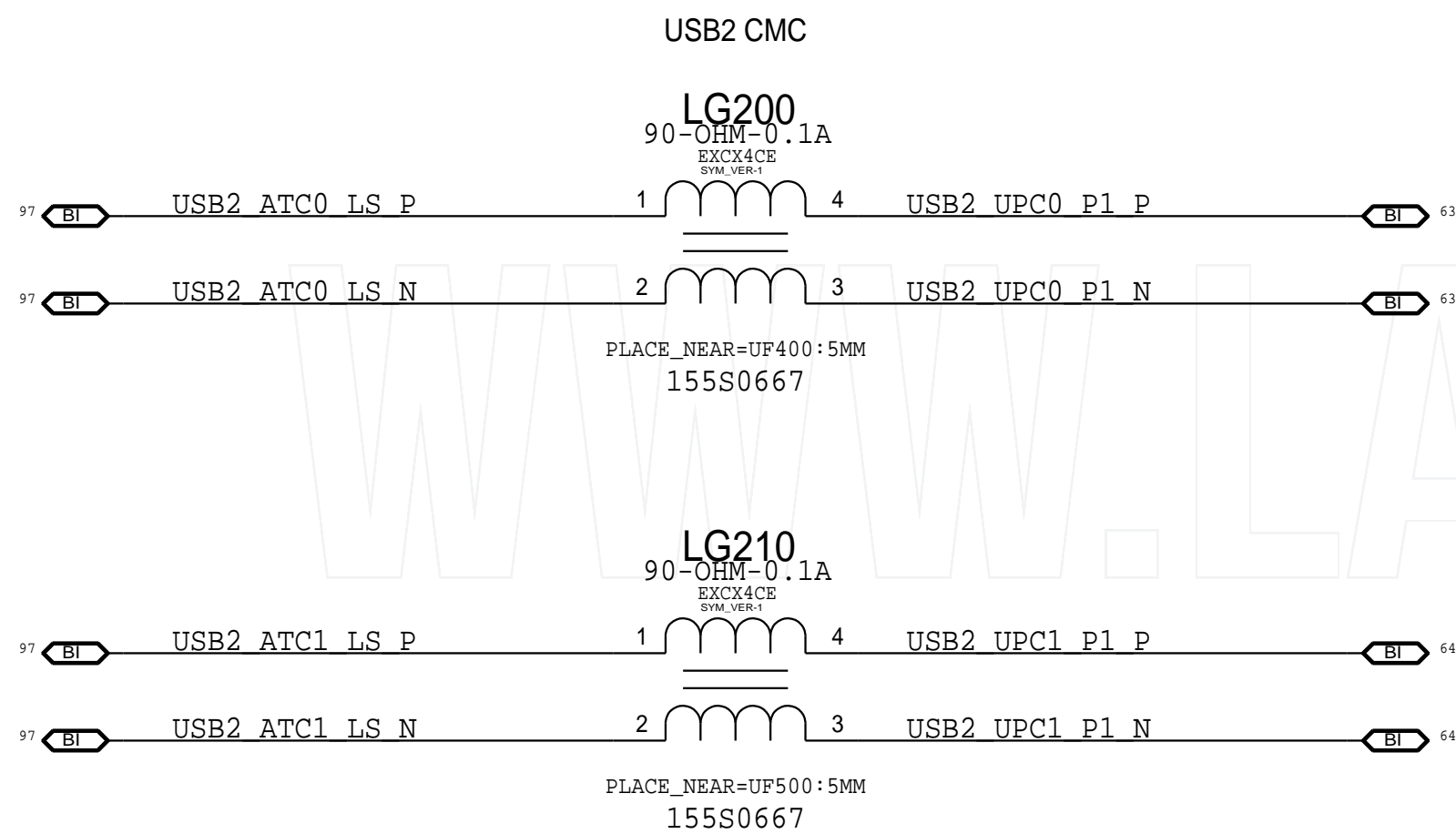
PAGE TITLE		
USB-C: HS Level Shifters		
	DRAWING NUMBER	051-07020
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A Charger AUX_DET Connections

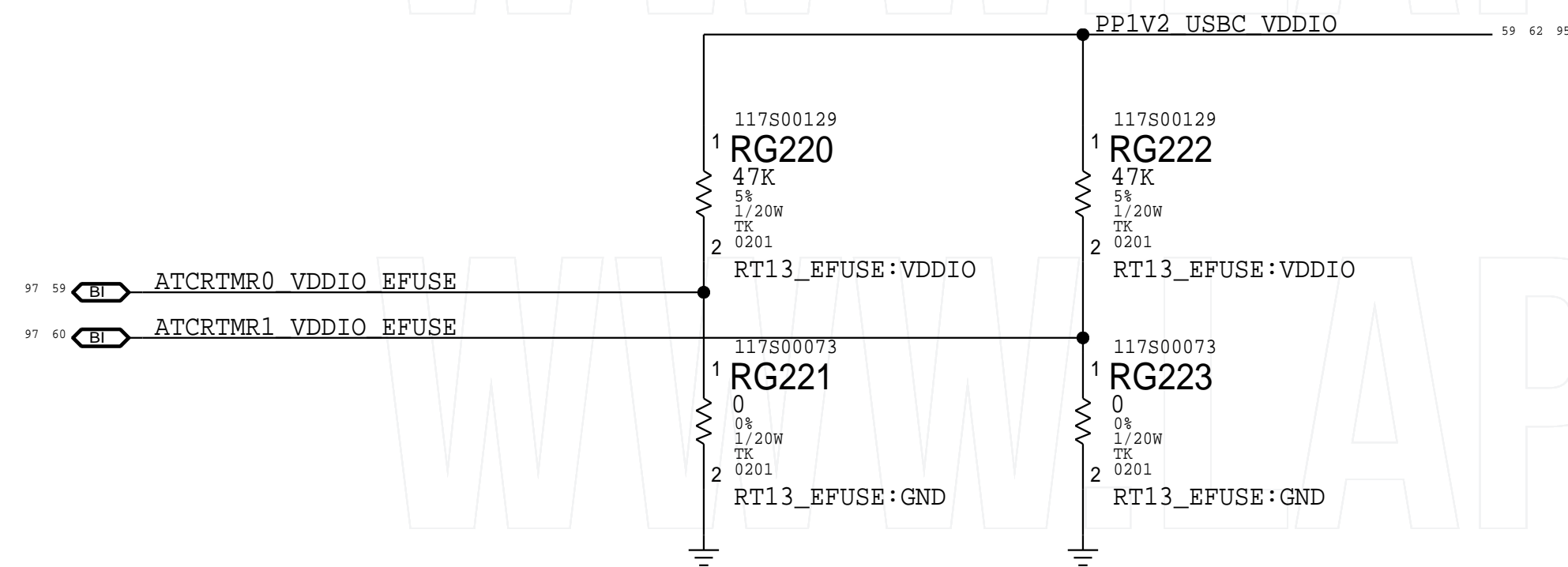
CHARGER AUX DET CONNECTIONS
<RDAR://70072178>
ALLOW ACE TO SEND A SIGNAL TO CHARGER
TO BLOCK SYSTEM CURRENT THROUGH ACE2 FETS DURING ACE2 SOFT START



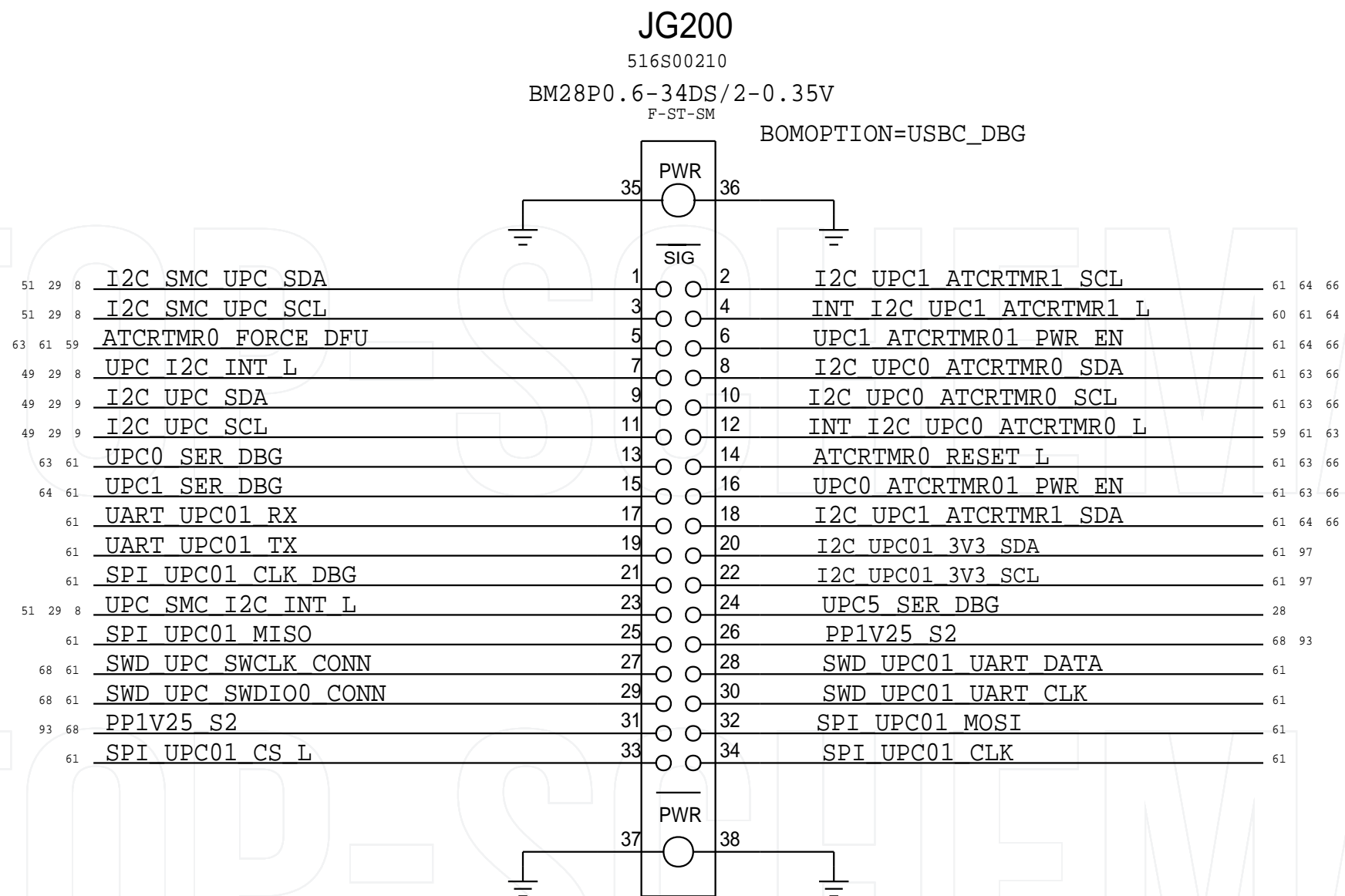
B USB 2.0 Common Mode Choke



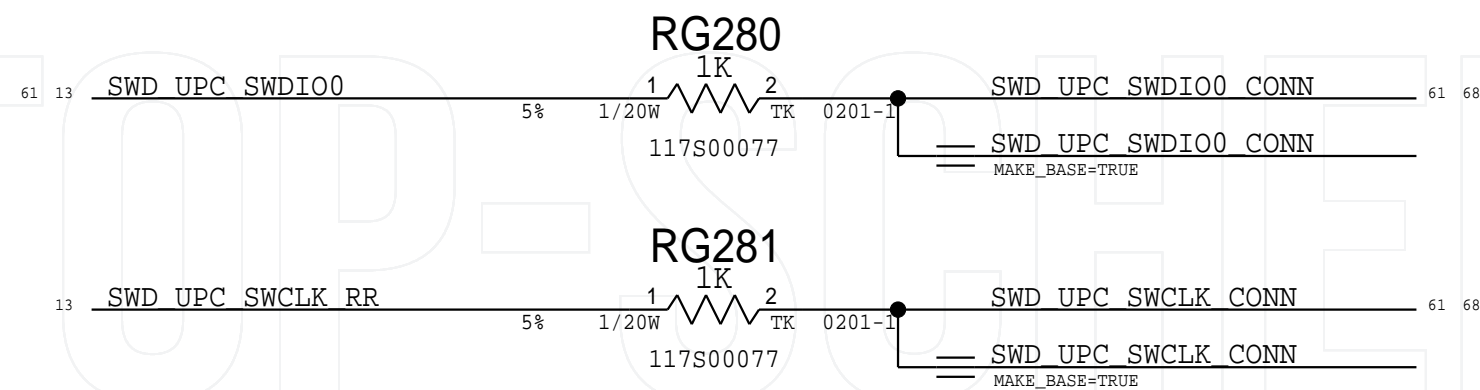
C RT13 VDDIO_EFUSE Selection



D USB-C/MagSafe Debug Connector



E USB-C SWDIO Aliases

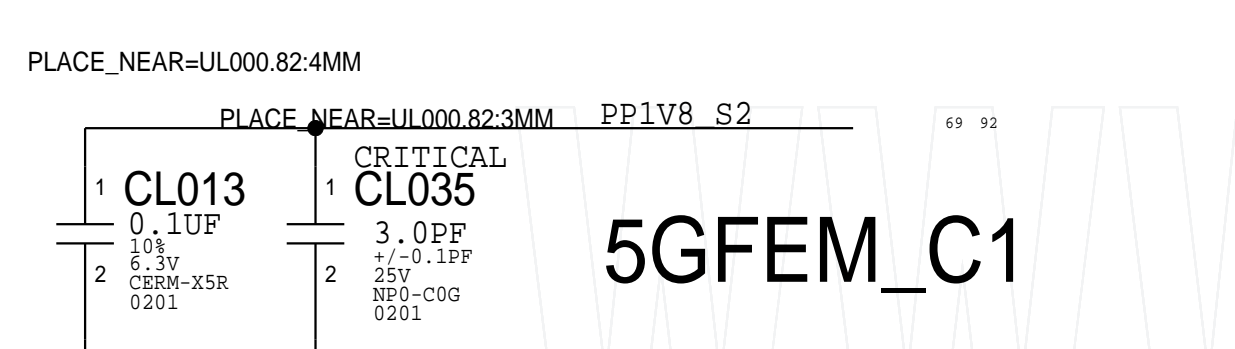
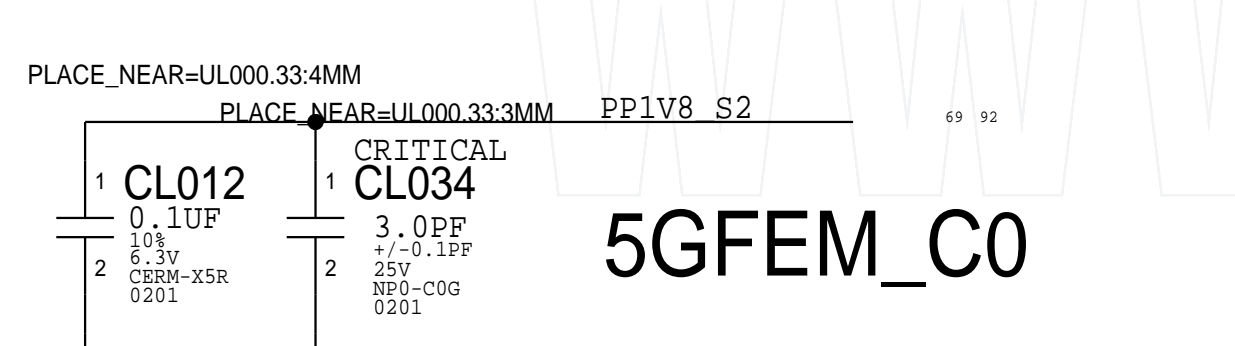
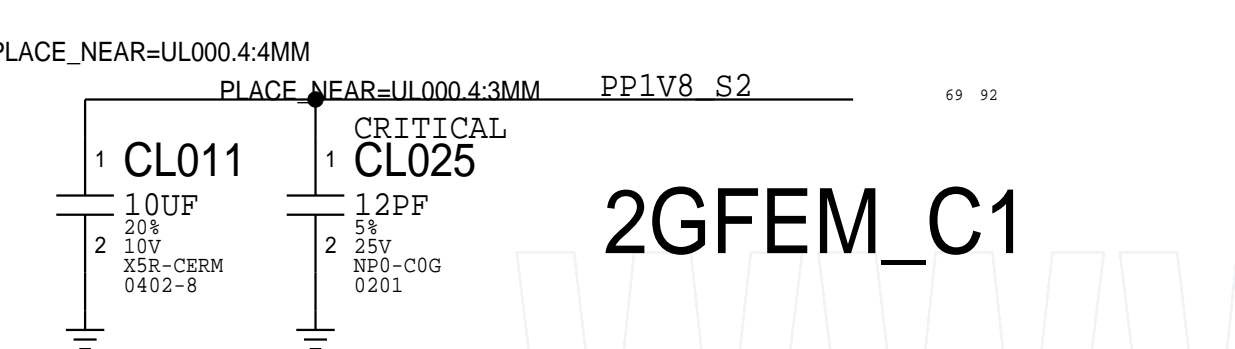
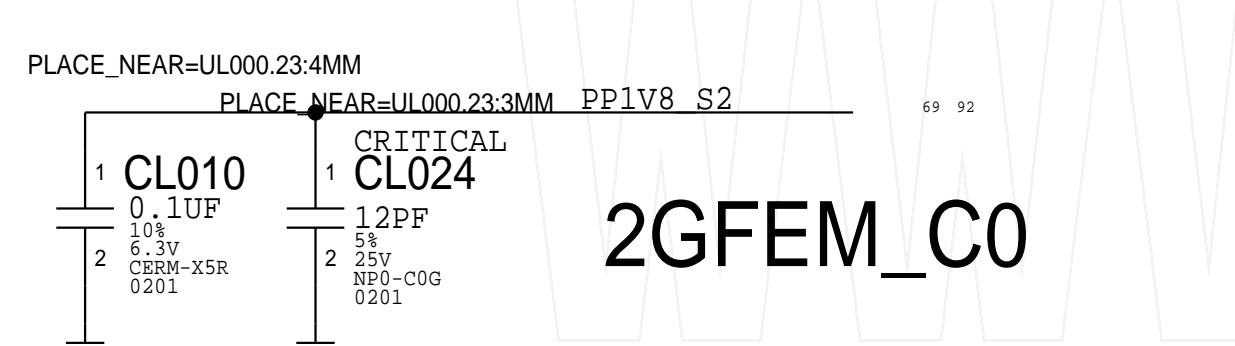
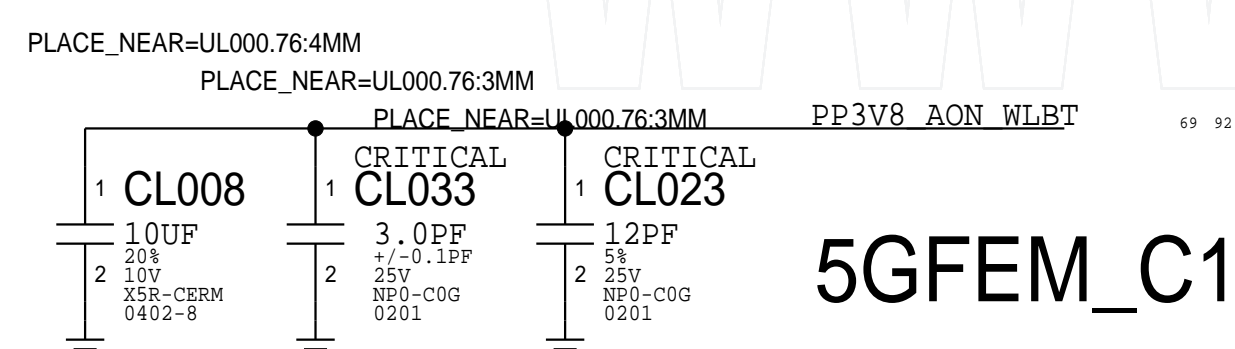
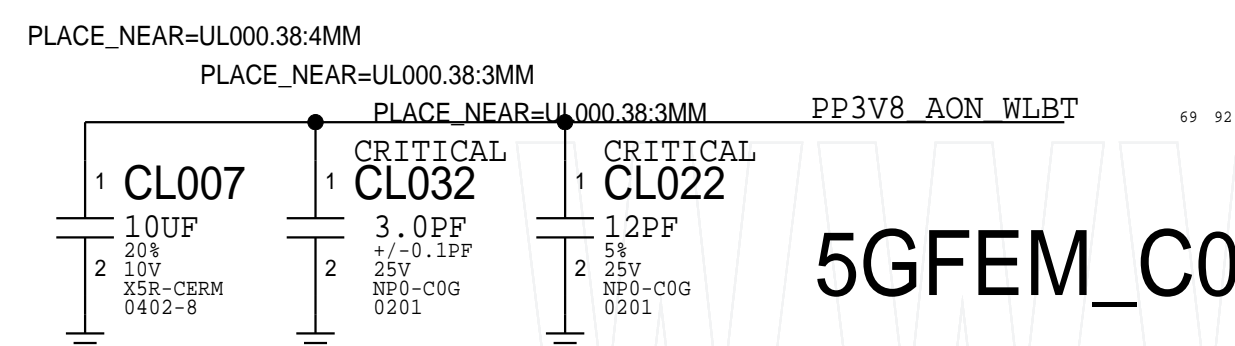
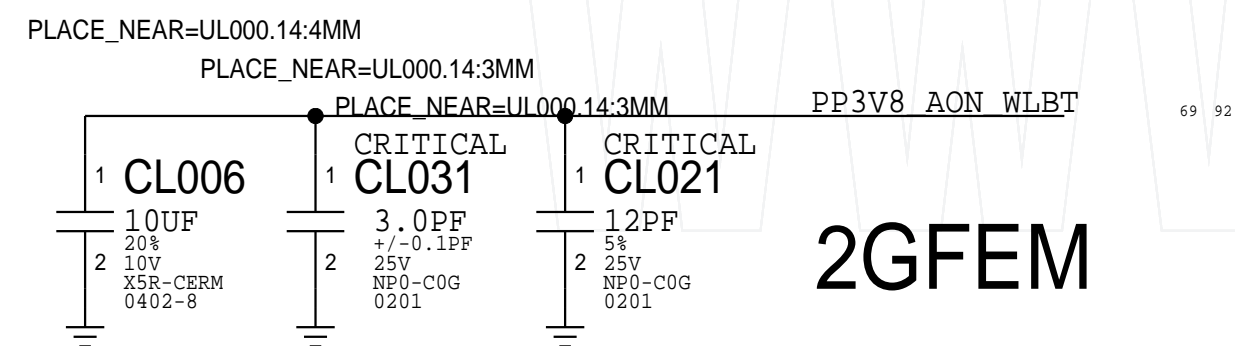
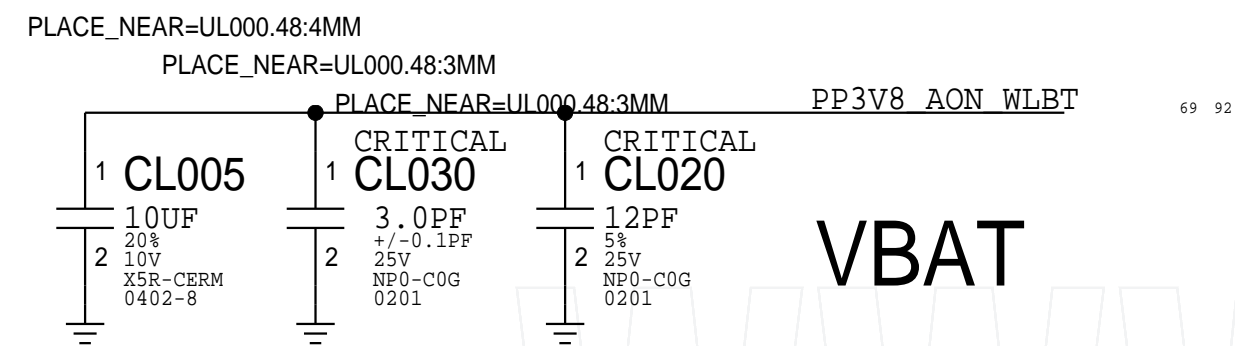


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USB-C: PROJECT SUPPORT		
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BOM_COST_GROUP=USB-C

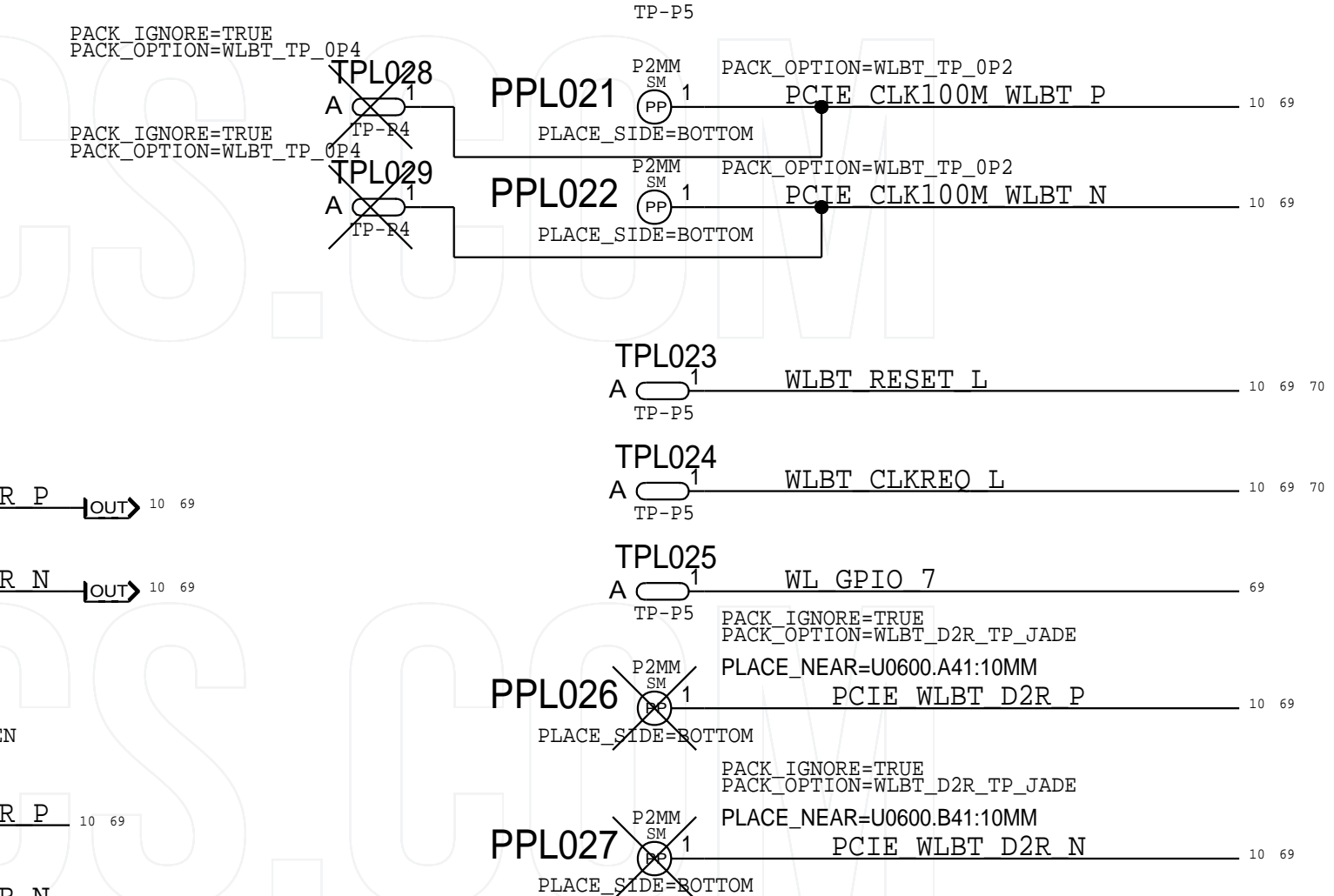
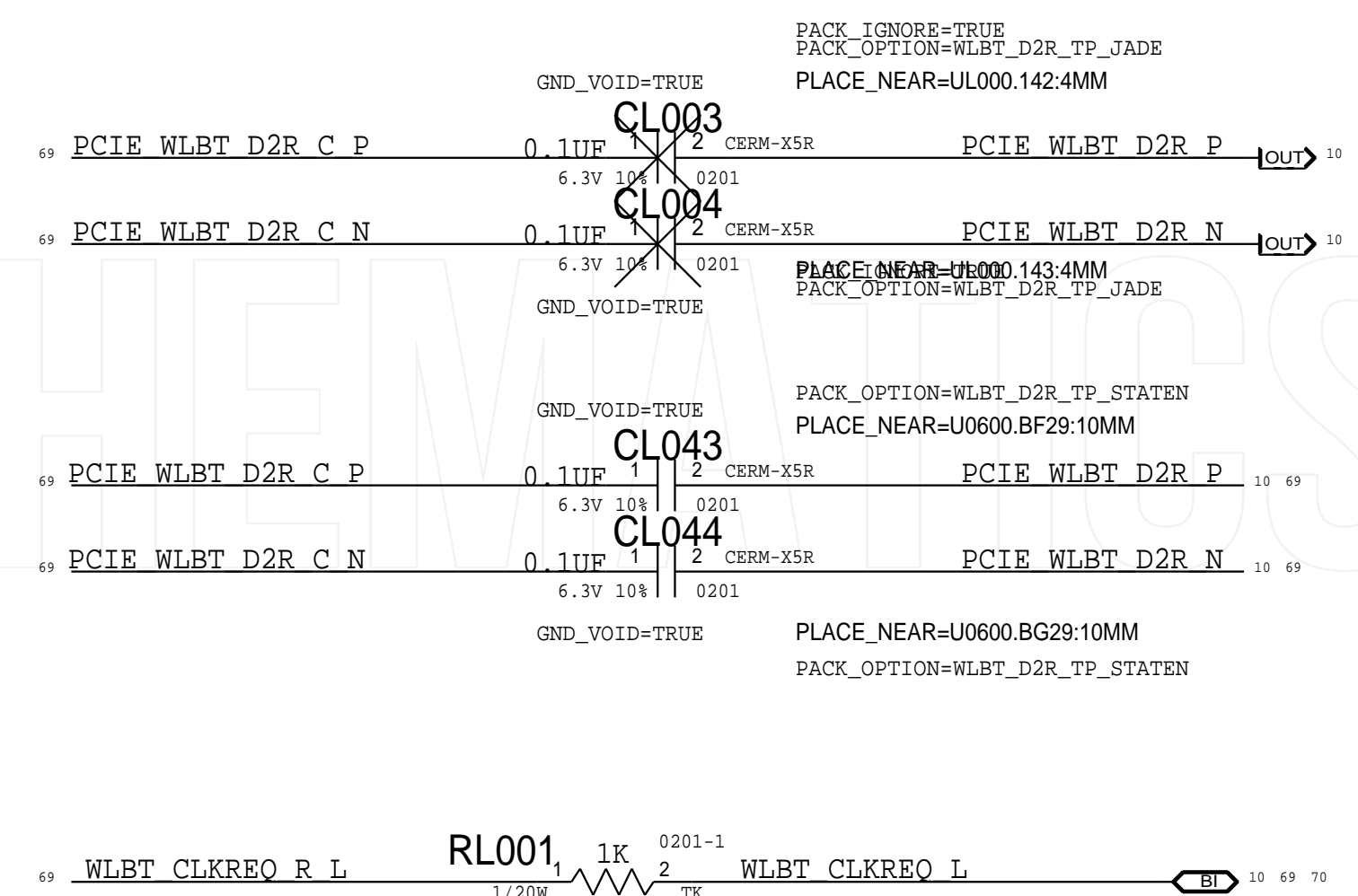
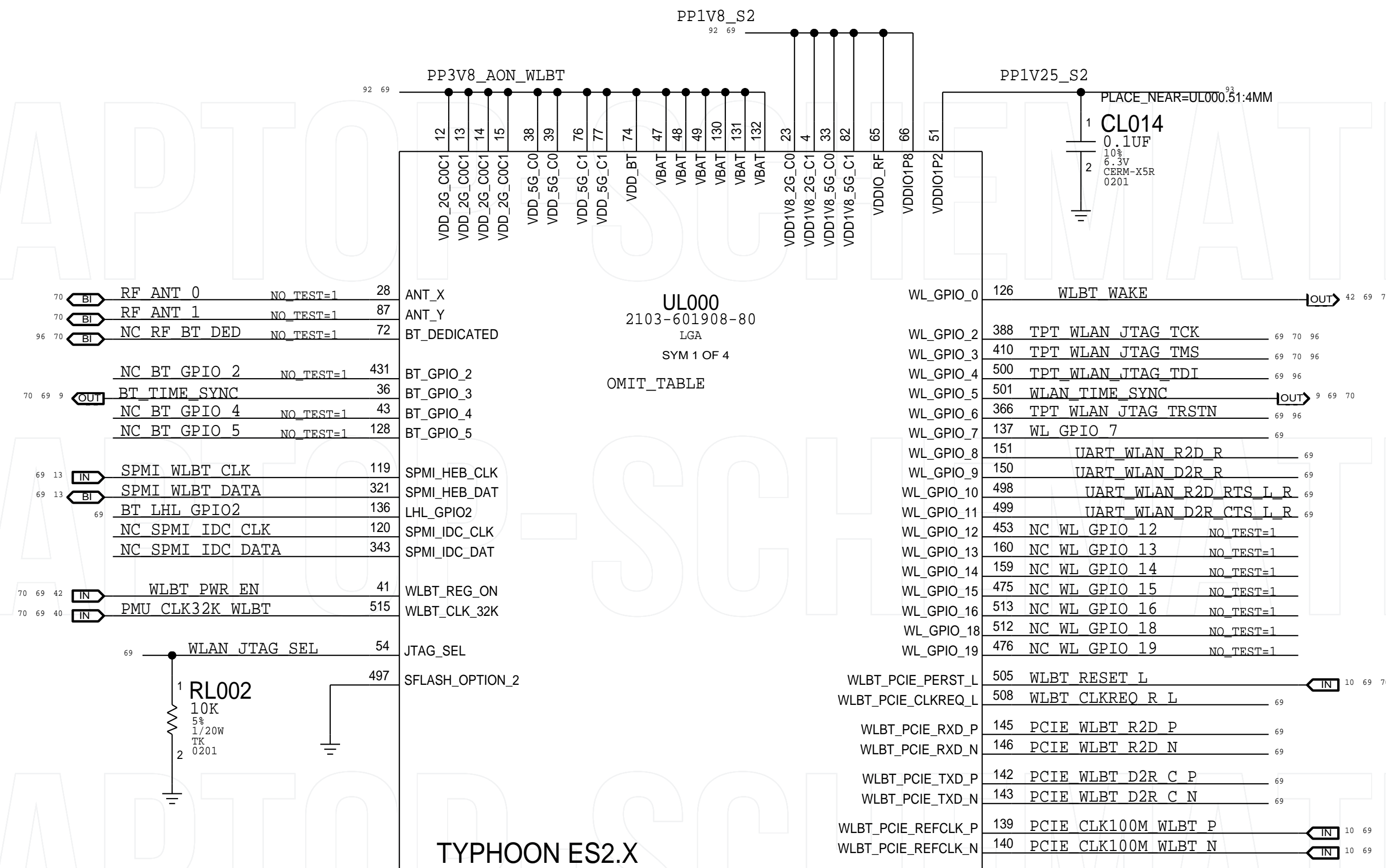
FOR SYSTEM INTEGRATION INFORMATION REFER TO
RDAR://PROBLEM/59047597


TYPHOON WIFI/BT MODULE



TYPHOON BOM TABLE:

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
339S00912	1	MODULE, WLAN/BT, TYPHOON, ES4.7	UL000	CRITICAL	



PAGE TITLE		WIFI/BT: MODULE	
 Apple Inc.	DRAWING NUMBER	051-07020	SIZE D
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	BRANCH	evt-1	
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	SHEET	69 OF 113	

TYPHOON WIFI/BT MODULE GND

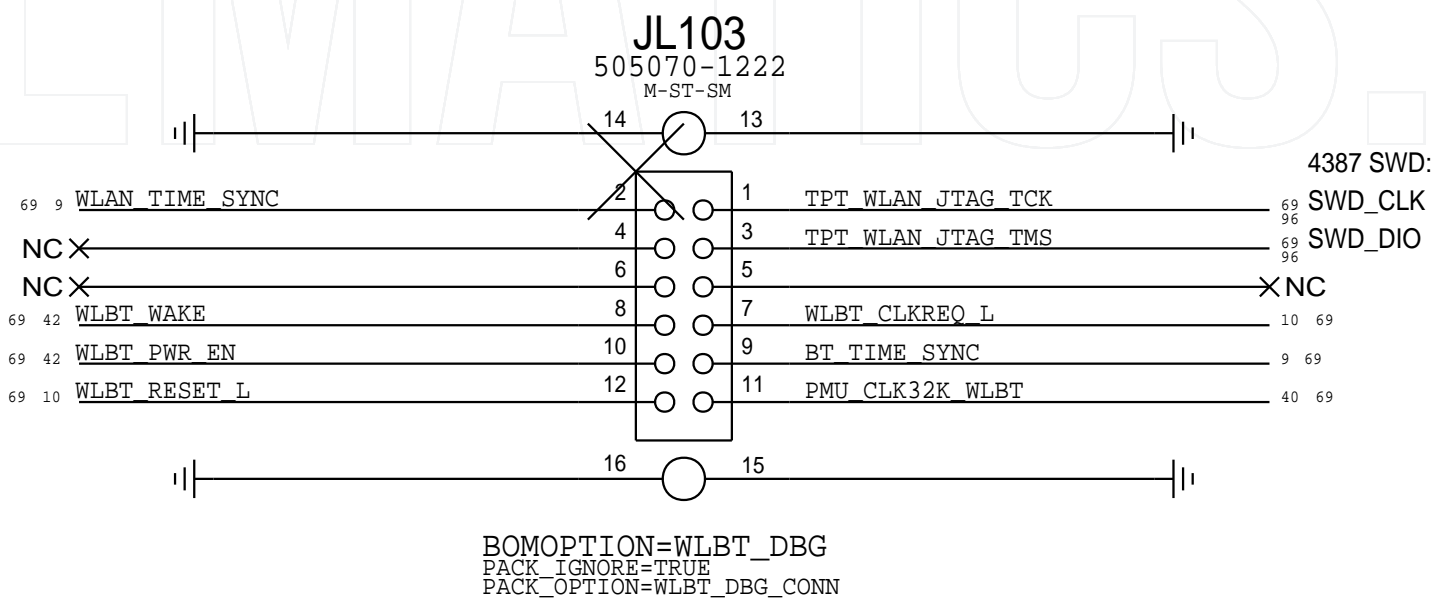
ANTENNA CONNECTORS

2G_C0
5G_C0
BT_C0

2G_C1
5G_C1
BT_C1

BT_C1_DED

WLBT DEBUG CONNECTOR



PAGE TITLE		
WIFI/BT: ANTENNA and GND		
	DRAWING NUMBER	051-07020
	REVISION	6.0.0
	BRANCH	evt-1
	PAGE	201 OF 801
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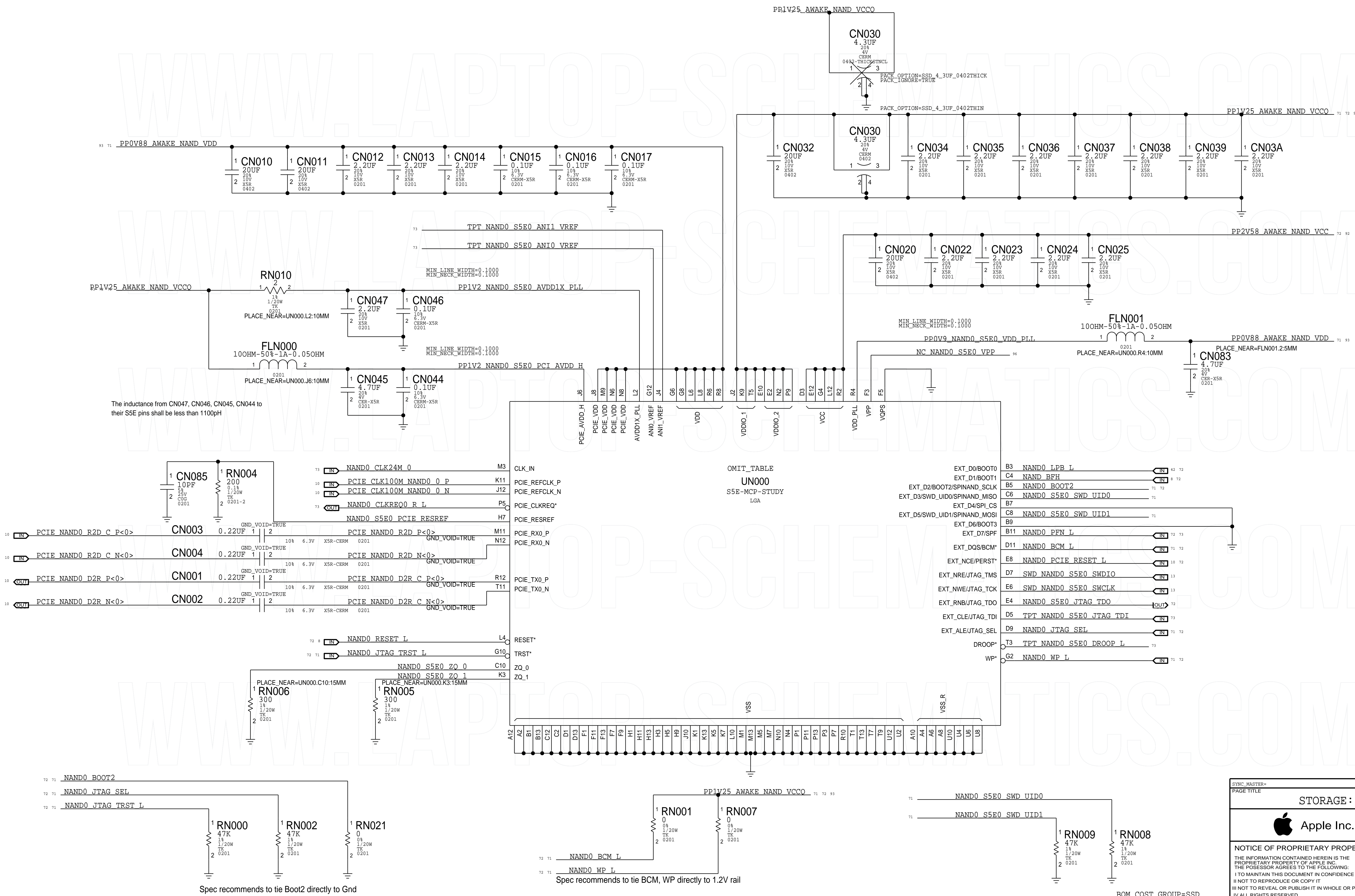
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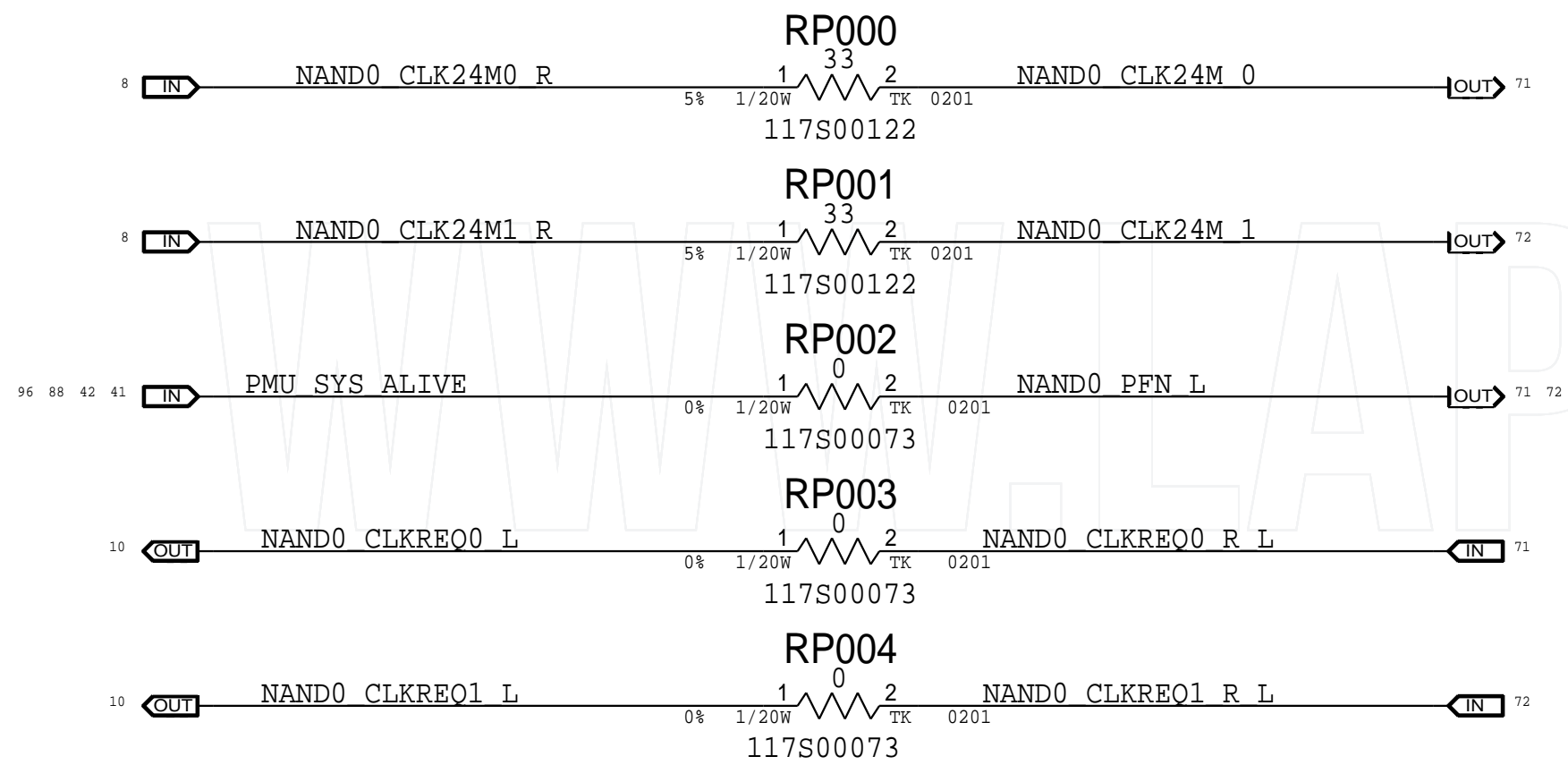
ASED 8BY WWW.LAPTOP-7SCHEMATIC

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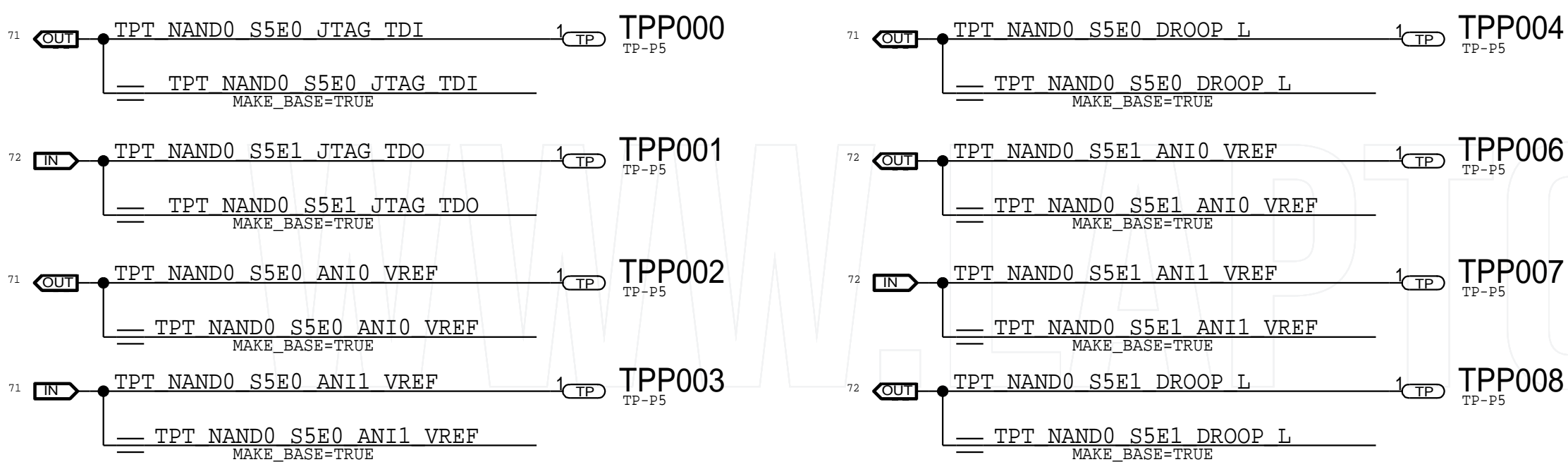


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		221 OF 801 SHEET			
		72 OF 113			

A SSD Termination Resistors



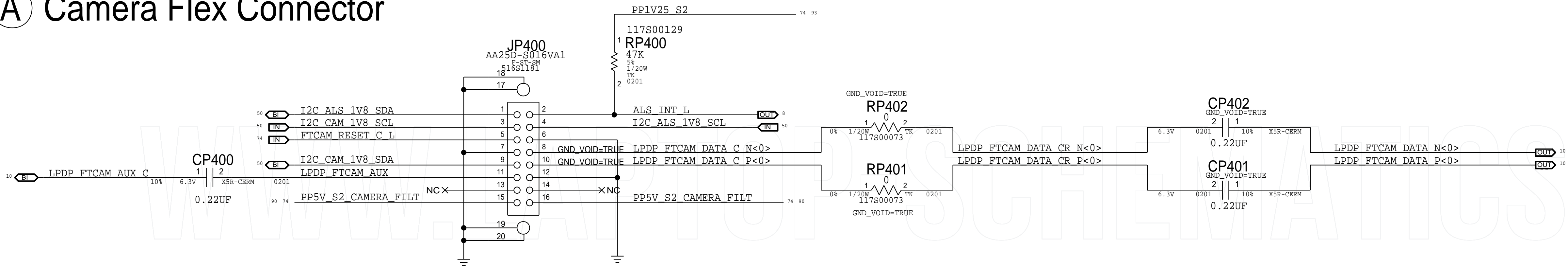
B S5E Test Points



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III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART			SHEET		
IV ALL RIGHTS RESERVED			73 OF 113		

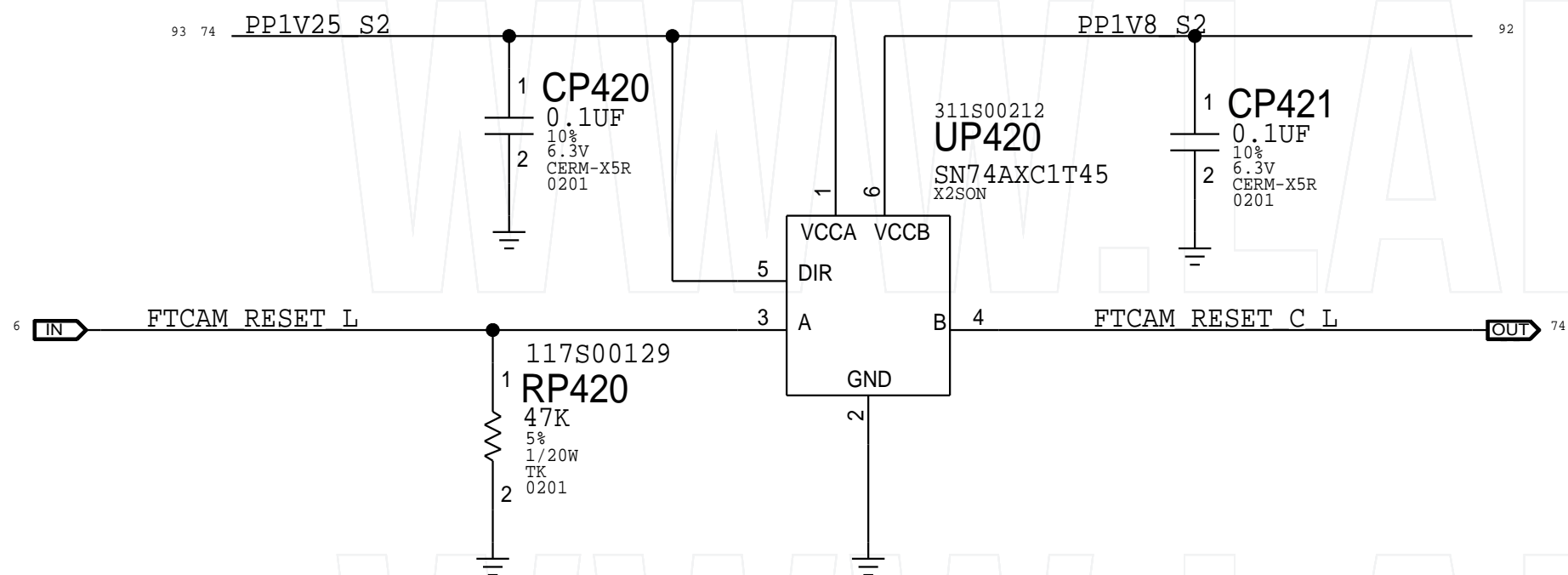
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A Camera Flex Connector

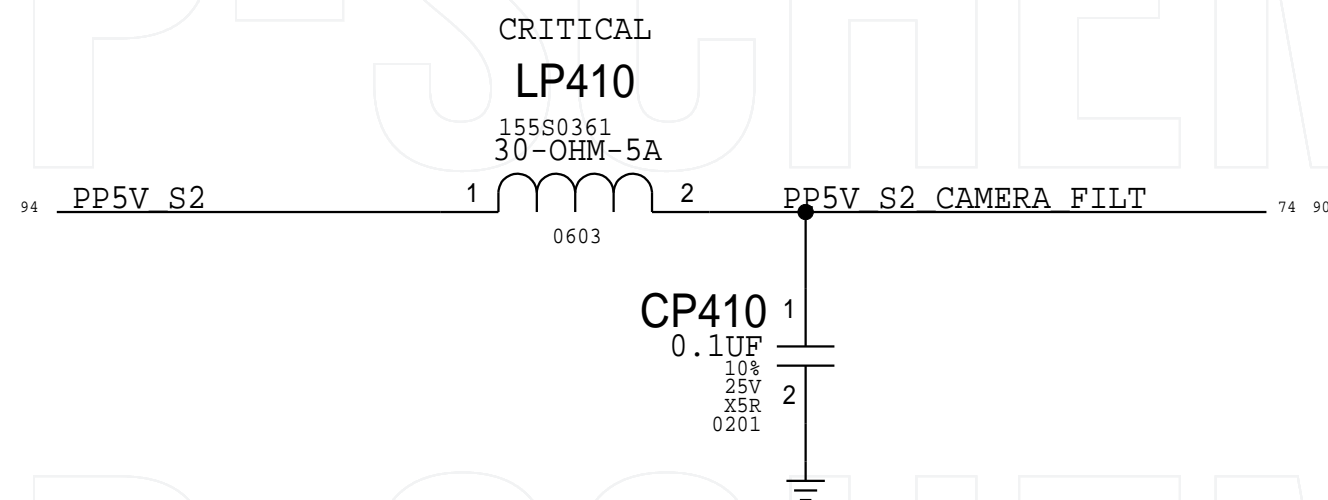


CAM TAIL FLEX CONNECTOR APN 516S1180

B Camera Reset Level Shifter



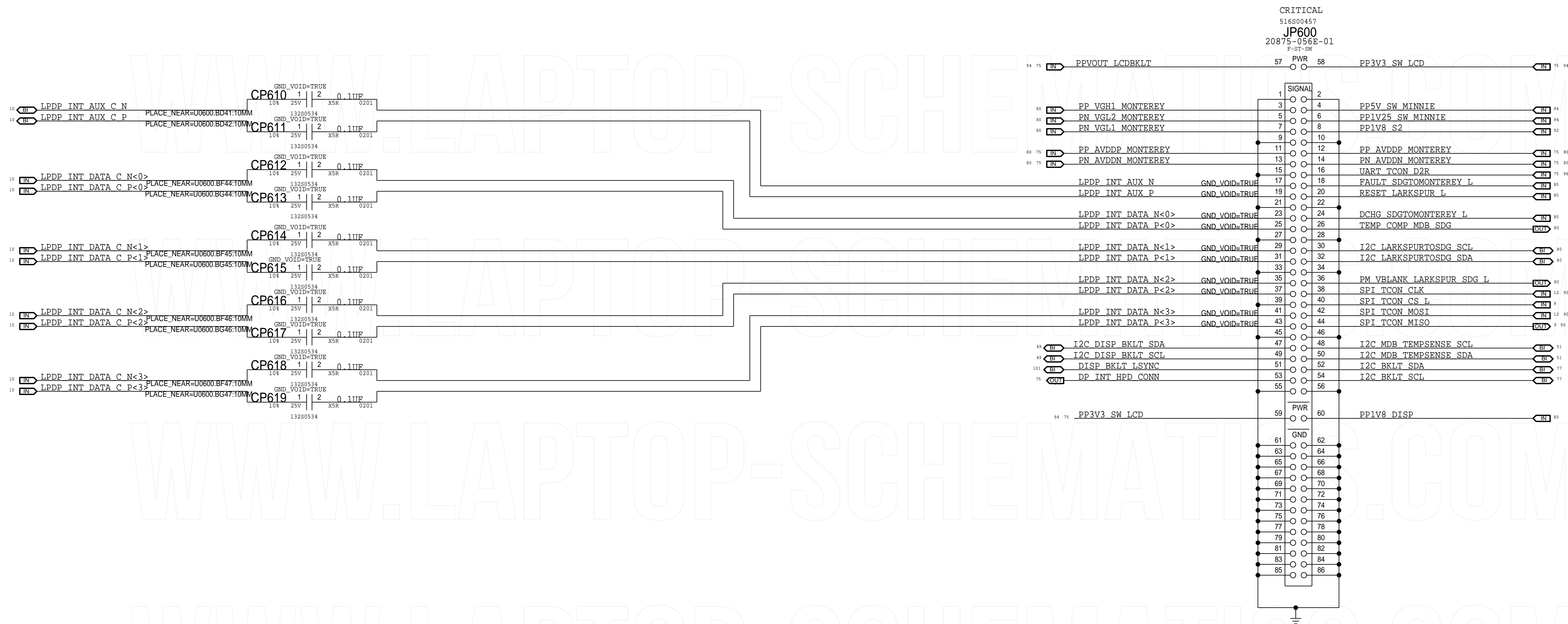
C Camera Power Filter(s)



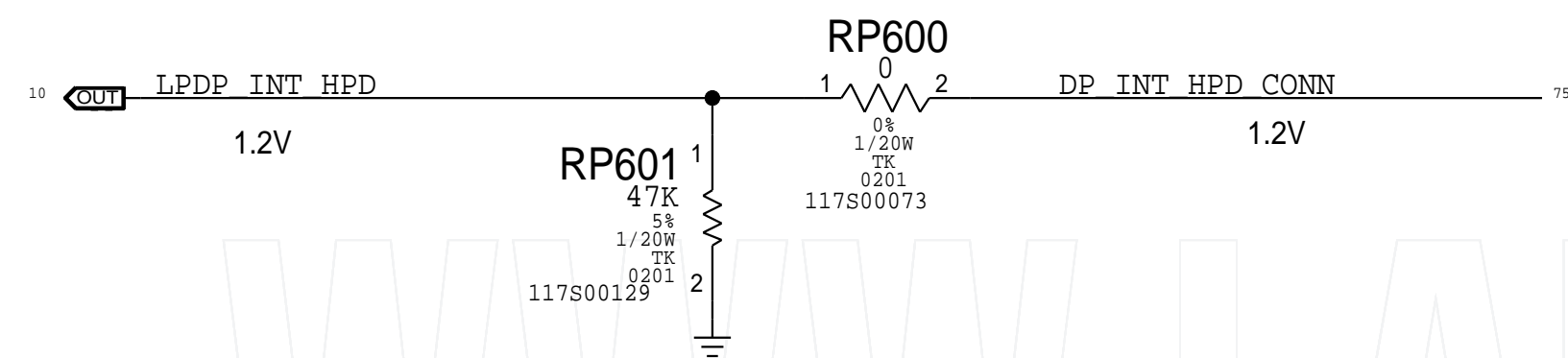
CAMERA: FLEX CONNECTOR		
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BOM_COST_GROUP=CAMERA

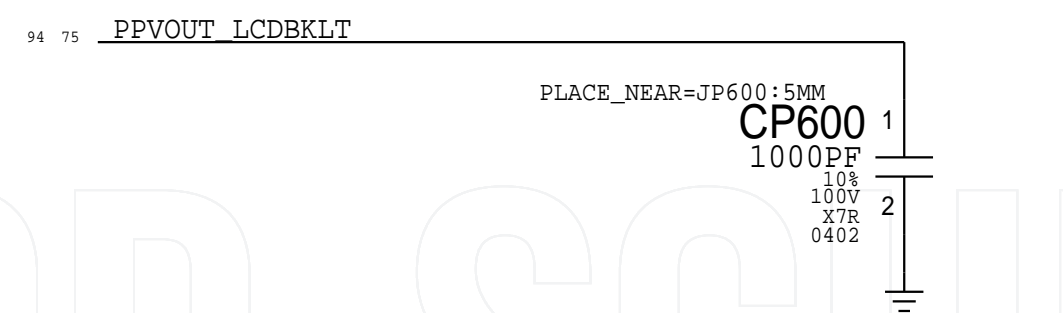
A LCD Panel Interface



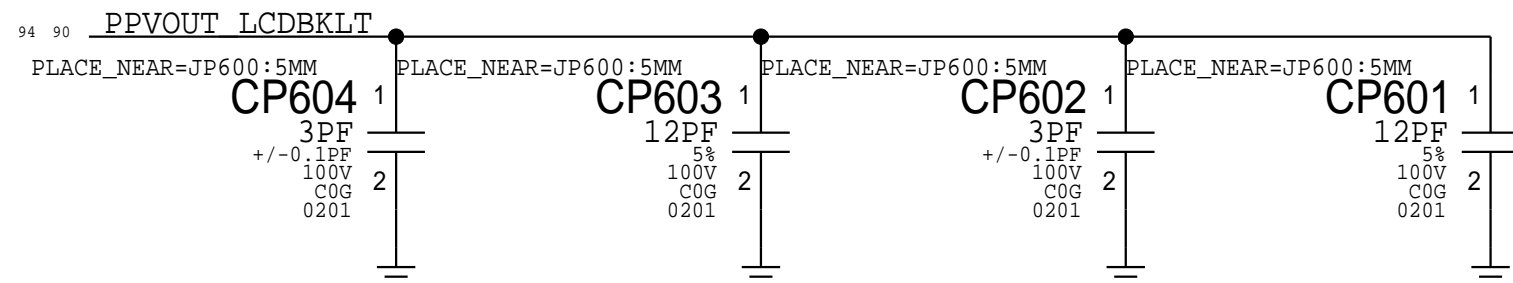
B LCD Panel Support



D LCD Panel Bypass



C LCD Panel Desense



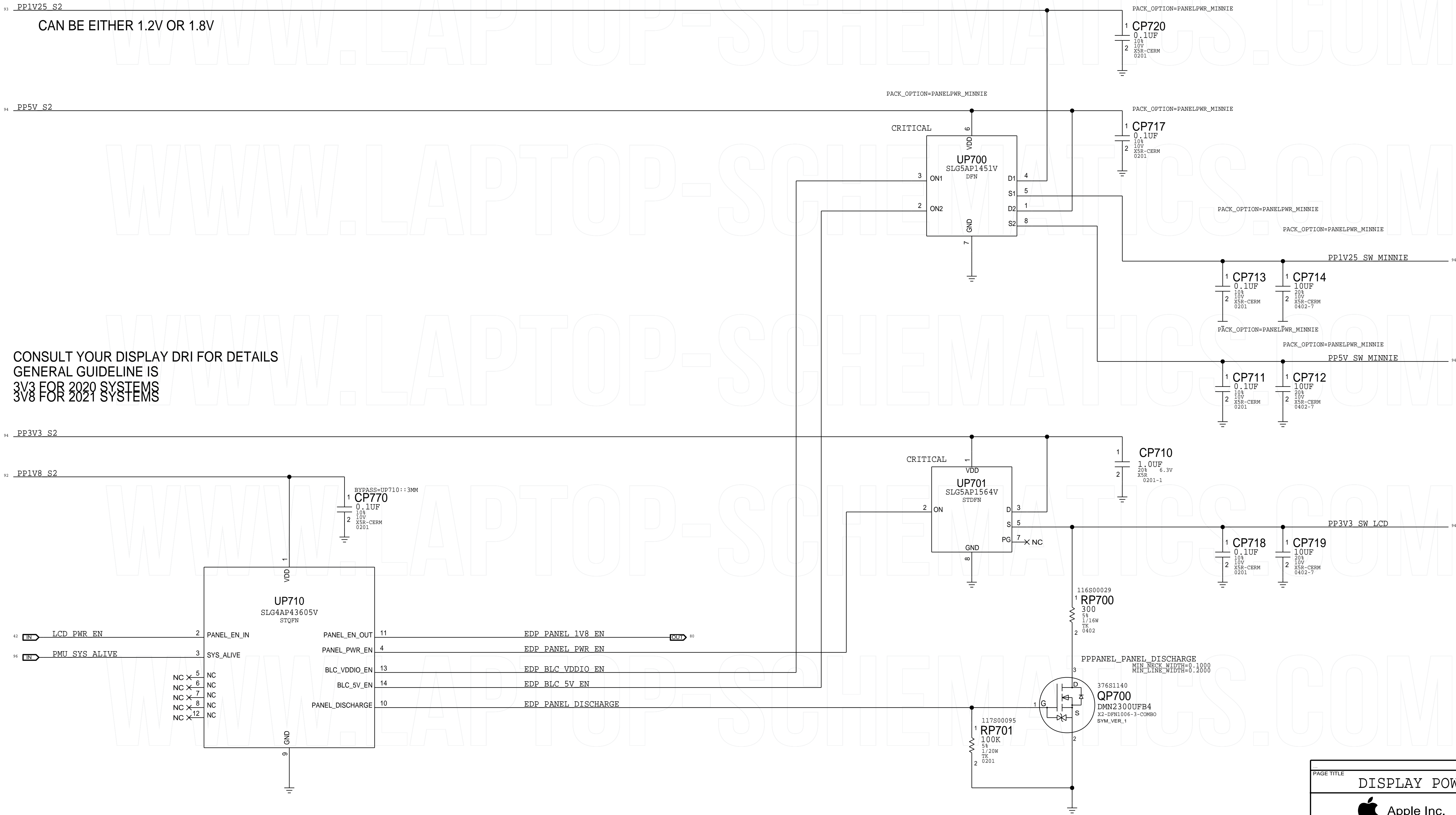
E UART PULLDOWN




eDP Display Connector		
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BOM_COST_GROUP=DISPLAY

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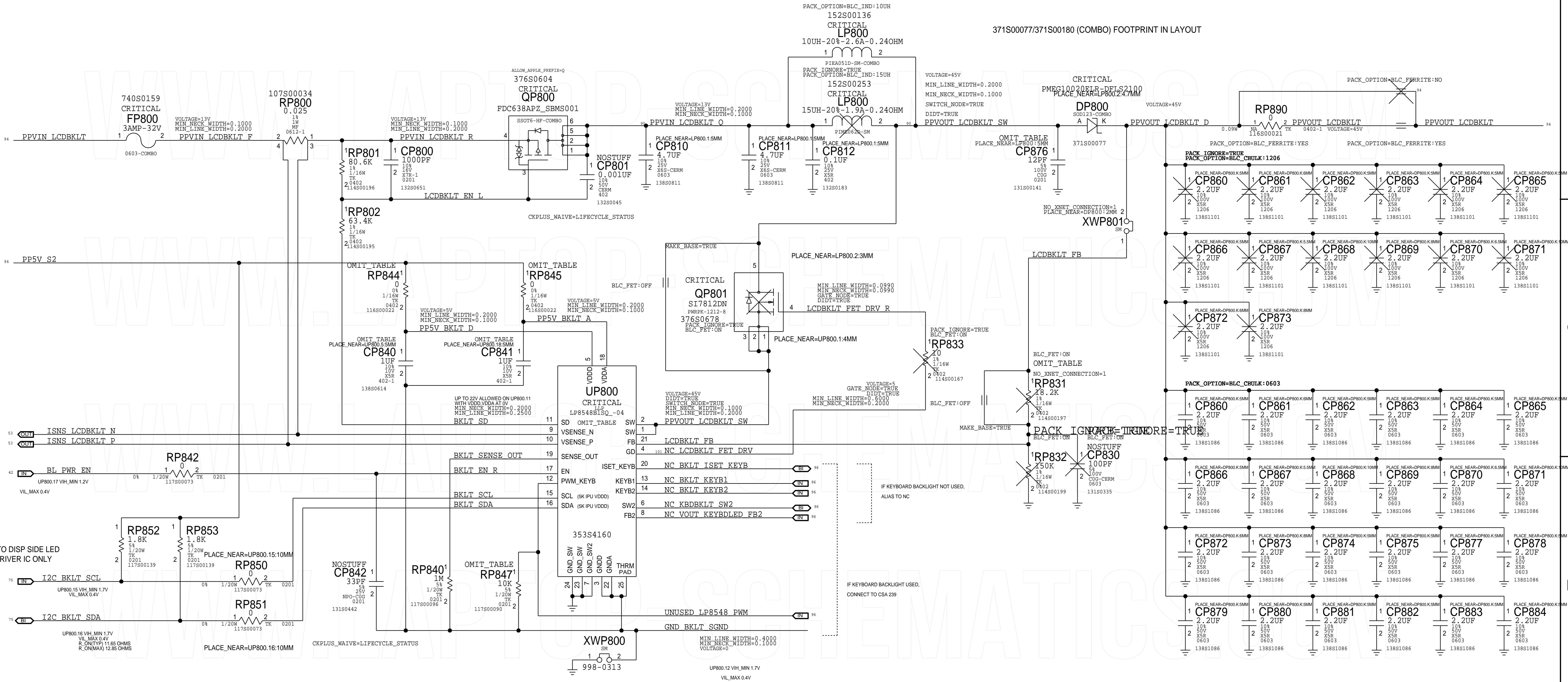


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DISPLAY POWER SEQUENCER		
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	PAGE	237 OF 801
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BOM_COST_GROUP=DISPLAY

BEN IC: DISPLAY/KBD BACKLIGHT BOOST CONVERTER

*** OK2INTEGRATE ***



BEN IC VERSION TO MATCH VERSION OF JERRY/MINNIE IC IS ON THE PANEL

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
35384160	1	IC, LP8548B1-04, DC/DC CVTR, BOOST, QFN-24	UP800		BLC_BEN_IC:V4
353802256	1	IC, LP8548B1A-07, DC/DC BOOST CVTR, QFN24	UP800		BLC_BEN_IC:V7
353802616	1	IC, LP8548B1A-08, DC/DC BOOST CVTR, QFN24	UP800		BLC_BEN_IC:V8

BACKLIGHT SWITCH NODE DESENSE OPTION

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
131800141	1	CAP, COG, 12PF, 5%, 100V, 0201	CP876		BLC_SW_NODE_DESENSE

10K IF KEYBOARD PWM INPUT IS NOT PRESENT (X841, X1536)
100K IF KEYBOARD PWM INPUT IS PRESENT (X1536)


PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
117800090	1	RES, TK, 10K OHM, 5%, 1/20W, 0201	RP847		BLC_KBD_BOOST_USED:NO
118800251	1	RES, TK, 100K OHM, 1%, 1/20W, 0201	RP847		BLC_KBD_BOOST_USED:YES

BACKLIGHT BOOST VOLTAGE LEVEL BASED ON NUMBER OF LEDS PER STRING

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
114800197	1	RES, TK, 18.2KOHM, 1%, 1/16W, 0402	RP831		BLC_LEDS_PER_STRING:16
114800198	1	RES, TK, 28.7KOHM, 1%, 1/16W, 0402	RP831		BLC_LEDS_PER_STRING:18

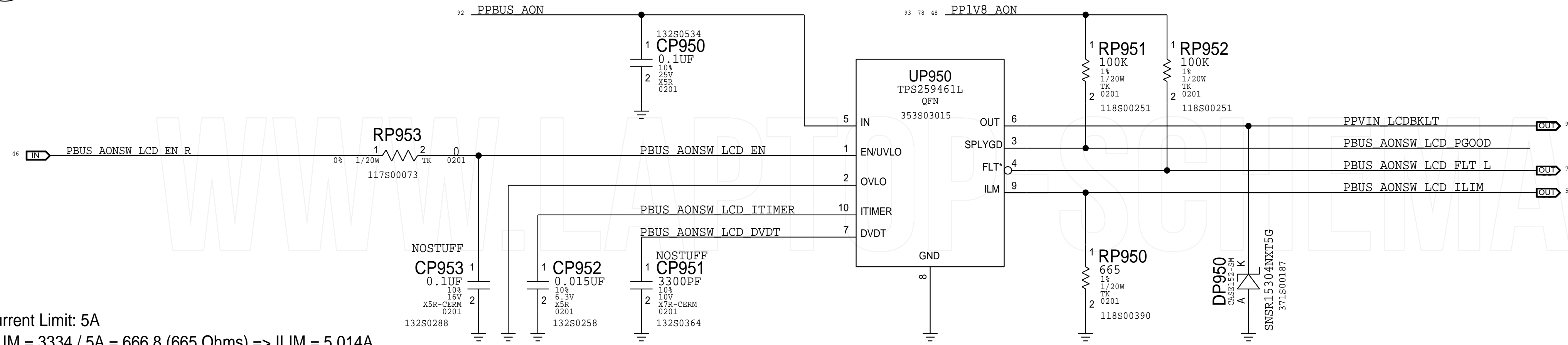
BOM OPTION FOR BLC 5V RC FILTER, BASED ON PER PROJECT 5V RIPPLE CHARACTERIZATION, AS COMPARED TO BLC TEAM'S 50 MV RIPPLE SPEC FOR VDDO & VDDA, SEE <RDAR://50682542>

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
116800022	2	RES, TK, 0 OHM, 2A MAX, 1/16W, 0402	RP844, RP845		BLC_5V_SERIES:0_OHM
114800167	2	RES, TK, 10 OHM, 1%, 1/16W, 0402	RP844, RP845		BLC_5V_SERIES:10_OHM
13880614	2	CAP, CER, X5R, 1UF, 10%, 10V, 0402	CP840, CP841		BLC_5V_CAP:1_1UF
138800070	2	CAP, CER, X5R, 4.7UF, 20%, 25V, 0402	CP840, CP841		BLC_5V_CAP:4P7_UF

SYNC_MASTER=DisplayBacklight		SYNC_DATE=09/26/2021	
PAGE TITLE			
BEN: CONTROLLER			
	Apple Inc.	DRAWING NUMBER	SIZE
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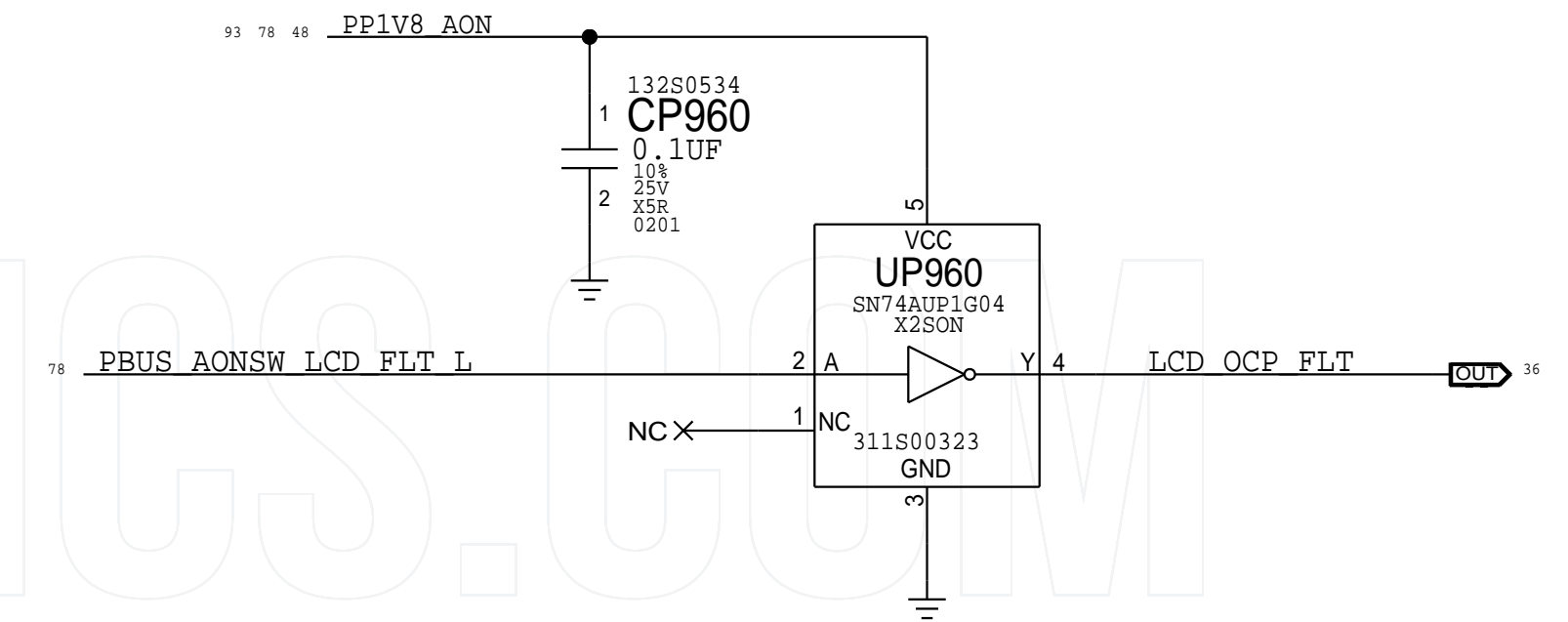
BOM_COST_GROUP=DISPLAY


Ⓐ PPBUS_AONSW_LCD Load Switch & e-Fuse



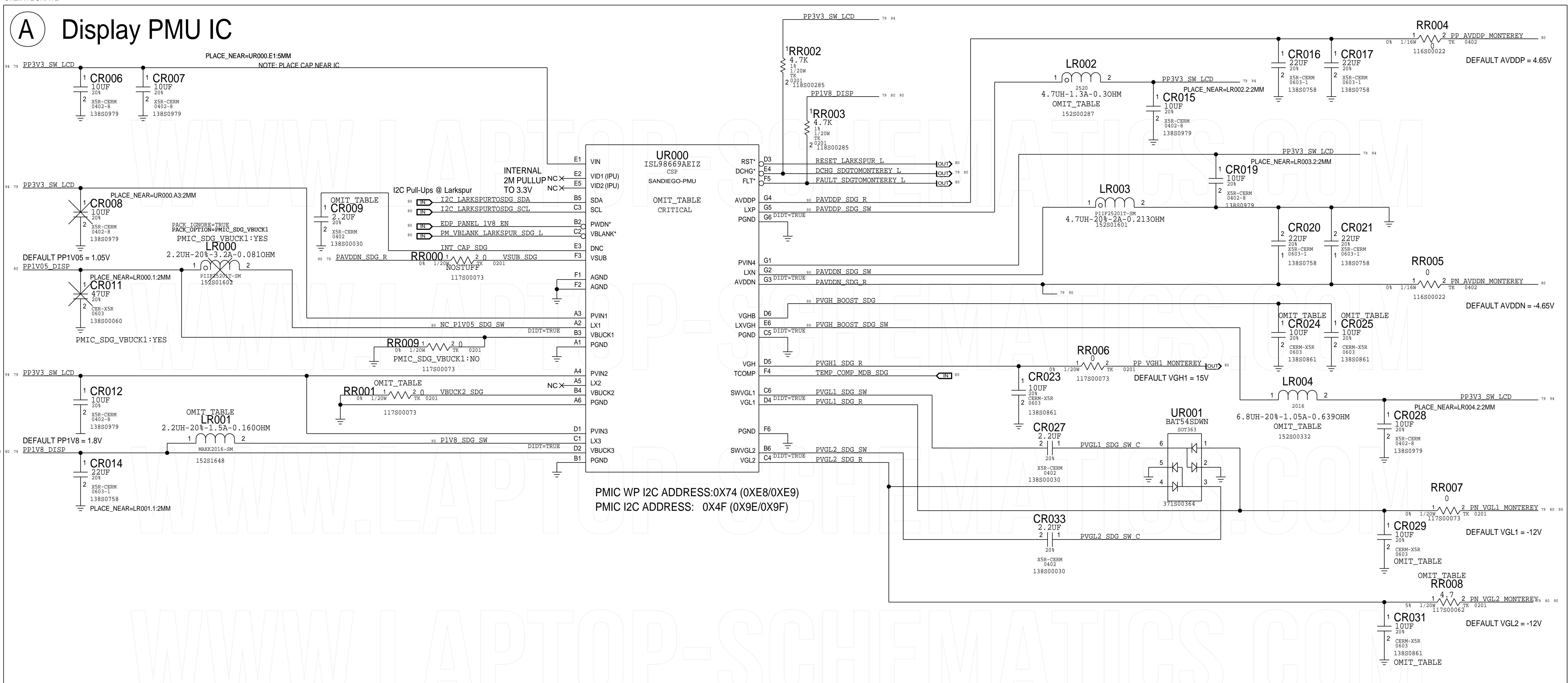
Current Limit: 5A
RLIM = 3334 / 5A = 666.8 (665 Ohms) => ILIM = 5.014A
/FLT Open Drain
Host-Controlled (EN = MPMU GPIO6, 1.8V LVC MOS (PP1V8_AON))

Ⓑ LCD_OCP_FLT Control Logic



SDC MASTER PAGE TITLE		DRAWING NUMBER 051-07020		DATE 09/10/2011	
BEN: PBUS E-Fuse				SIZE D	
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A Display PMU IC



B BOMOPTIONS: TI vs. Intersil

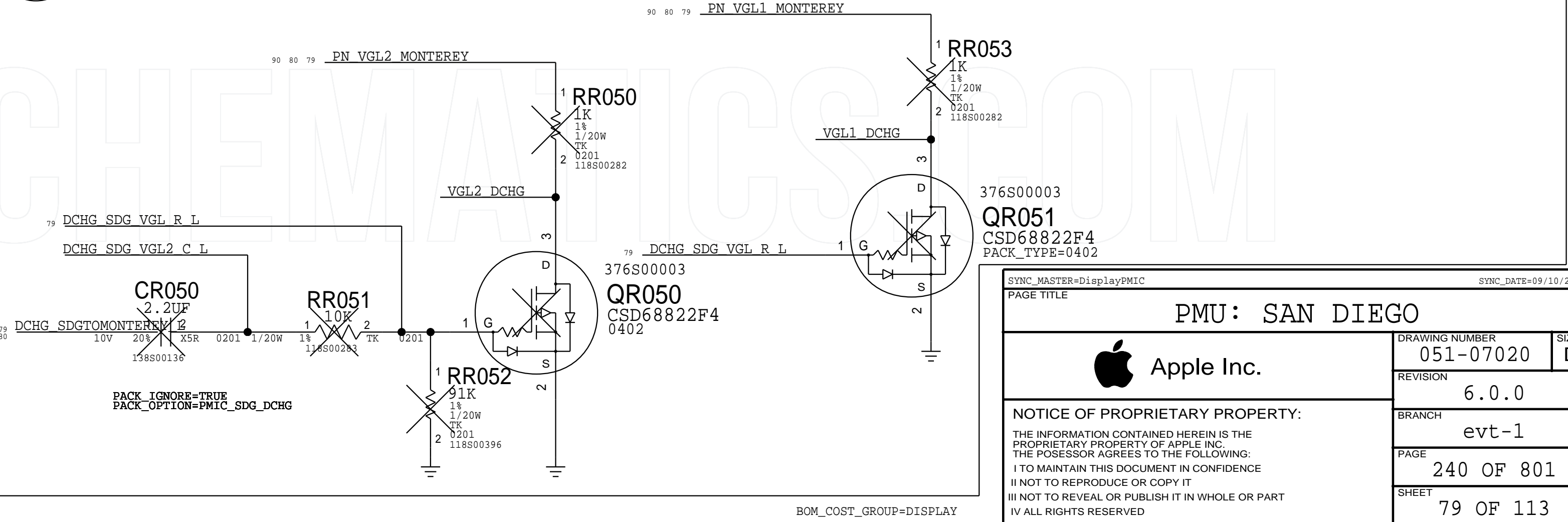
Texas Instruments Option Table

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
338S00844	1	IC,TP86515780B2,PMU,SAN DIEROD,A1,DSBGA42	UR000	SDG_TI_PROG:X2203
338S00185	1	IC,TP865157,SAN DIEROD,A1,DSBGA42	UR000	SDG_TI_PROG:BLANK
152S00289	2	IND,4.7UH,2016,PTA20161T-487WDR	LR001	SDG_TI
152S01601	1	IND,MLD,4.7UH,2016,2A,0.2130HM,2520	LR002	SDG_TI
152S00332	1	IND,6.8UH,2016,PISA20161T88-013	LR004	SDG_TI
138S0861	2	CAP,CER,10UF,20A,35V,XSR,0603	CR029,CR031	SDG_TI
138S0861	2	CAP,CER,10UF,20A,35V,XSR,0603	CR024,CR025	SDG_TI
138S00030	1	CAP,CER,2.2UF,20A,35V,XSR,0402	CR009	SDG_TI
117S00073	1	RES,TX,0 OHM,1A MAX,1/20W,0201	RR008	SDG_TI

Intersil Option Table

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
338S00183	1	IC,ISL98669,SAN DIEROD,A3,CSP42	UR000	SDG_ISL
152S1648	2	IND,2.2UH,2016,MAKK2016T282M	LR001	SDG_ISL
152S00286	1	IND,2.2UH,2520,VLS252010H8K-2R2M	LR002	SDG_ISL
152S00483	1	IND,1.0UH,2016,LQEM20160M0G0	LR004	SDG_ISL
138S0709	2	CAP,CER,4.7UF,10A,35V,XSR,0603	CR029,CR031	SDG_ISL
138S0709	2	CAP,CER,4.7UF,10A,35V,XSR,0603	CR024,CR025	SDG_ISL
116S00022	1	RES,0 OHM,1A,0402	CR009	SDG_ISL
117S00062	1	RES,TX,4.7 OHM,5A,1/20W,0201	RR008	SDG_ISL
117S00073	1	RES,TX,0 OHM,1A MAX,1/20W,0201	RR001	SDG_ISL

C PN_VGL1 & PN_VGL2 Discharge Circuit



PMU: SAN DIEGO

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A


Power Connections Alias

75	<u>PP1V8_DISP</u> MAKE_BASE=TRUE	==	<u>PP1V8_DISP</u>	79	90
	<u>PP1V05_DISP</u> MAKE_BASE=TRUE	==	<u>PP1V05_DISP</u>	79	
75	<u>PN_VGL1_MONTEREY</u> MAKE_BASE=TRUE	==	<u>PN_VGL1_MONTEREY</u>	79	90
75	<u>PN_VGL2_MONTEREY</u> MAKE_BASE=TRUE	==	<u>PN_VGL2_MONTEREY</u>	79	90
75	<u>PP_AVDDP_MONTEREY</u> MAKE_BASE=TRUE	==	<u>PP_AVDDP_MONTEREY</u>	79	
75	<u>PN_AVDDN_MONTEREY</u> MAKE_BASE=TRUE	==	<u>PN_AVDDN_MONTEREY</u>	79	
75	<u>PP_VGH1_MONTEREY</u> MAKE_BASE=TRUE	==	<u>PP_VGH1_MONTEREY</u>	79	
	<u>NC_P1V05_SDG_SW</u> MAKE_BASE=TRUE	==	<u>NC_P1V05_SDG_SW</u>	79	

B

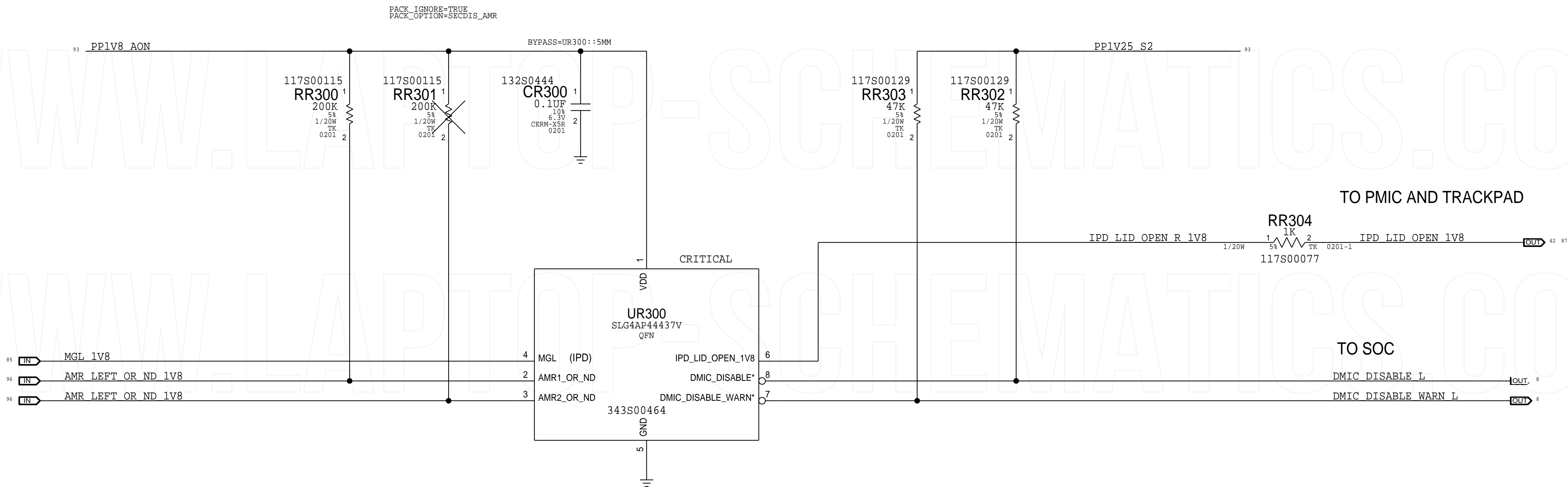
Signal Connections Alias

75	<u>I2C_LARKSPURTOSDG_SDA</u> MAKE_BASE=TRUE CXP105_HA1VE+I2C_PULLUP I2C Pull-Up @ Larkspur	==	<u>I2C_LARKSPURTOSDG_SDA</u>	79	
75	<u>I2C_LARKSPURTOSDG_SCL</u> MAKE_BASE=TRUE CXP105_HA1VE+I2C_PULLUP I2C Pull-Up @ Larkspur	==	<u>I2C_LARKSPURTOSDG_SCL</u>	79	
76	<u>EDP_PANEL_1V8_EN</u> MAKE_BASE=TRUE	==	<u>EDP_PANEL_1V8_EN</u>	79	
75	<u>PM_VBLANK_LARKSPUR_SDG_L</u> MAKE_BASE=TRUE	==	<u>PM_VBLANK_LARKSPUR_SDG_L</u>	79	
75	<u>RESET_LARKSPUR_L</u> MAKE_BASE=TRUE	==	<u>RESET_LARKSPUR_L</u>	79	
75	<u>DCHG_SDGTONTEREY_L</u> MAKE_BASE=TRUE	==	<u>DCHG_SDGTONTEREY_L</u>	79	
75	<u>FAULT_SDGTONTEREY_L</u> MAKE_BASE=TRUE	==	<u>FAULT_SDGTONTEREY_L</u>	79	
	<u>TEMP_COMP_MDB_SDG</u> MAKE_BASE=TRUE	==	<u>TEMP_COMP_MDB_SDG</u>	79	

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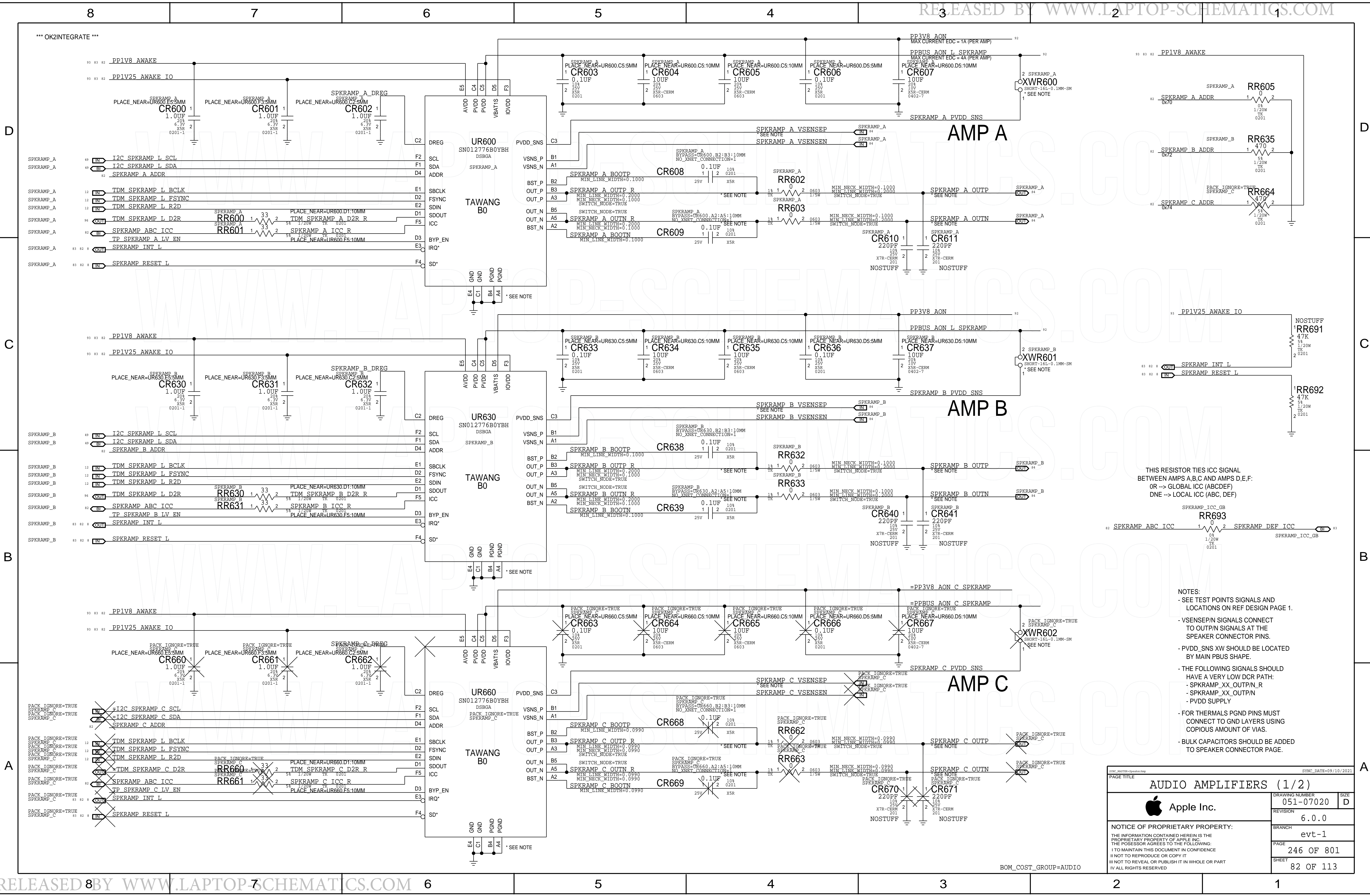
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LID SECDIS LOGIC



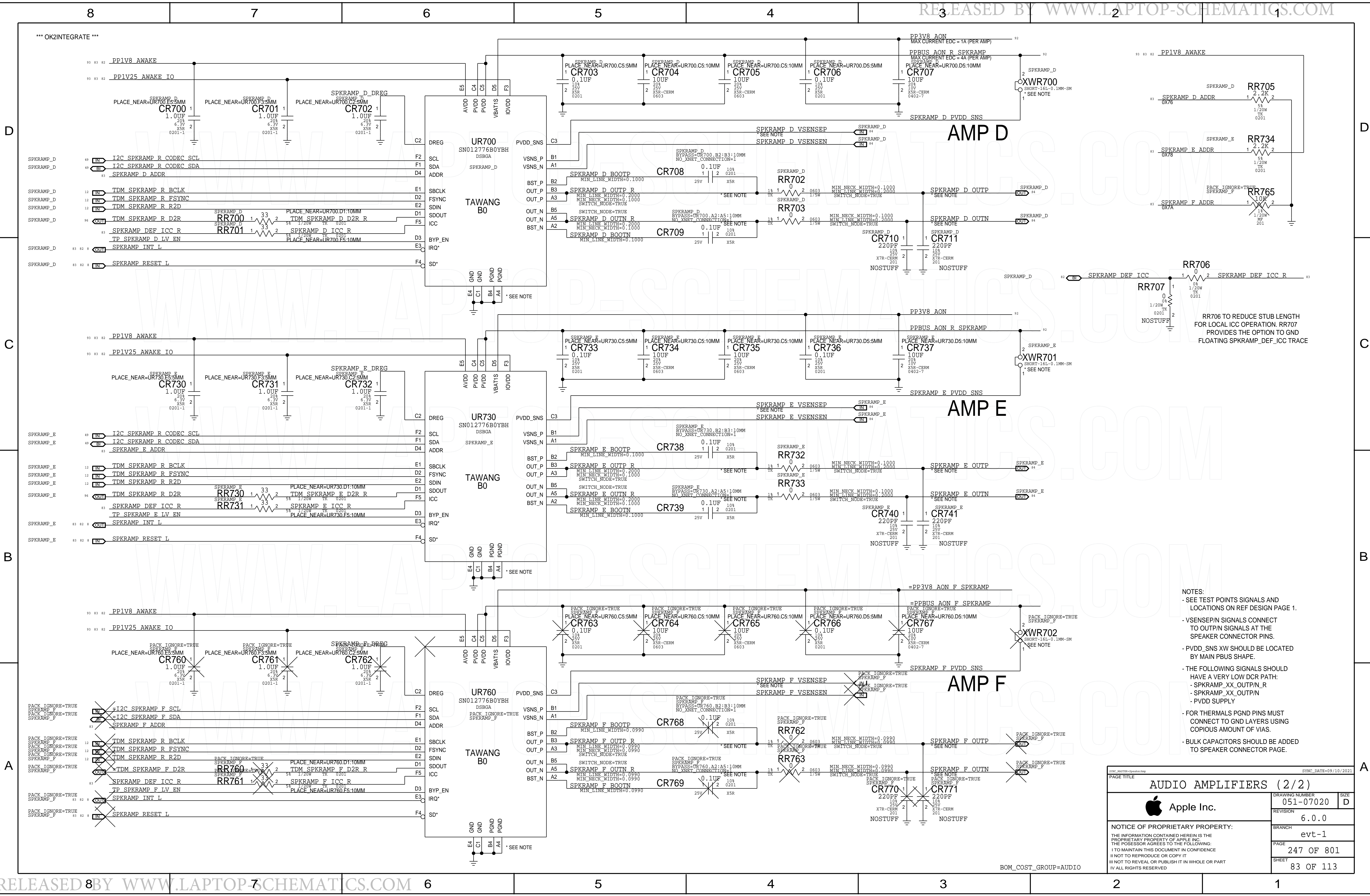
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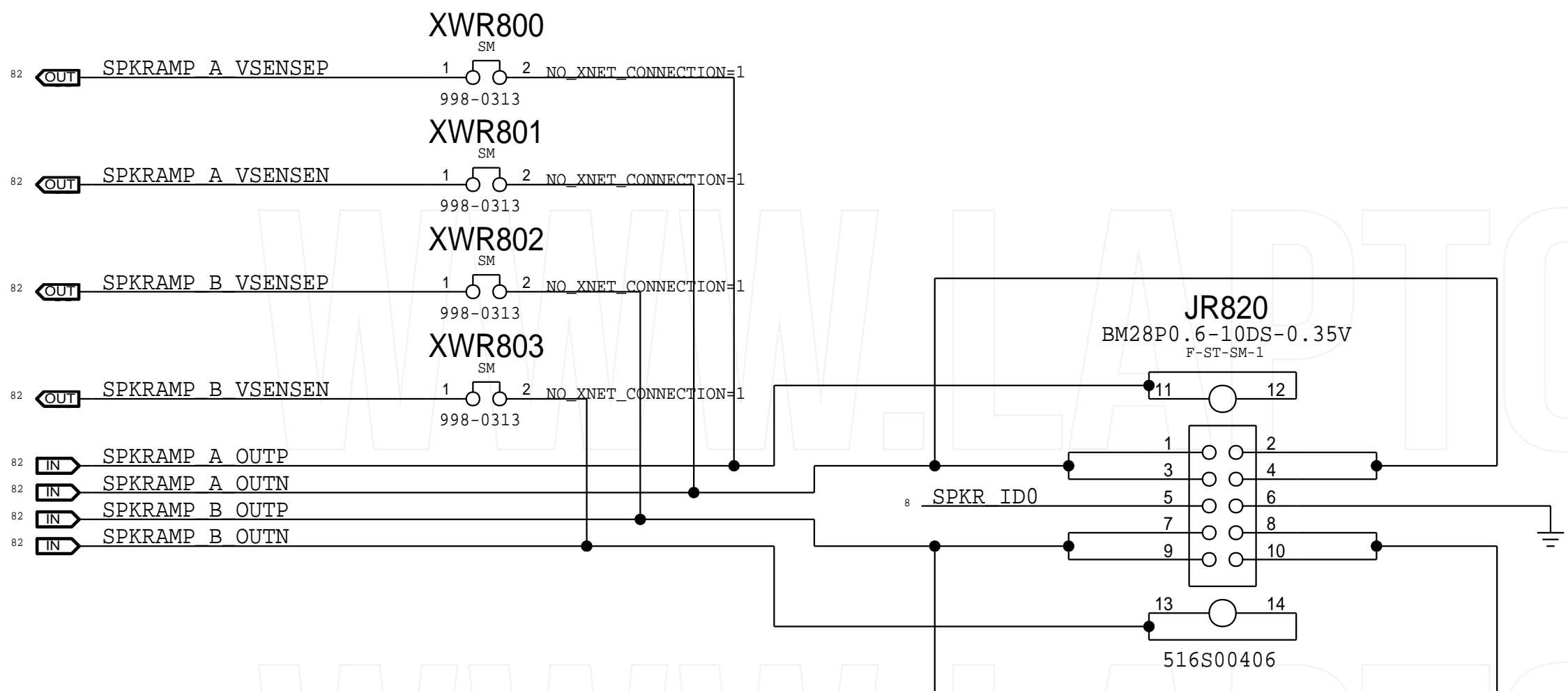
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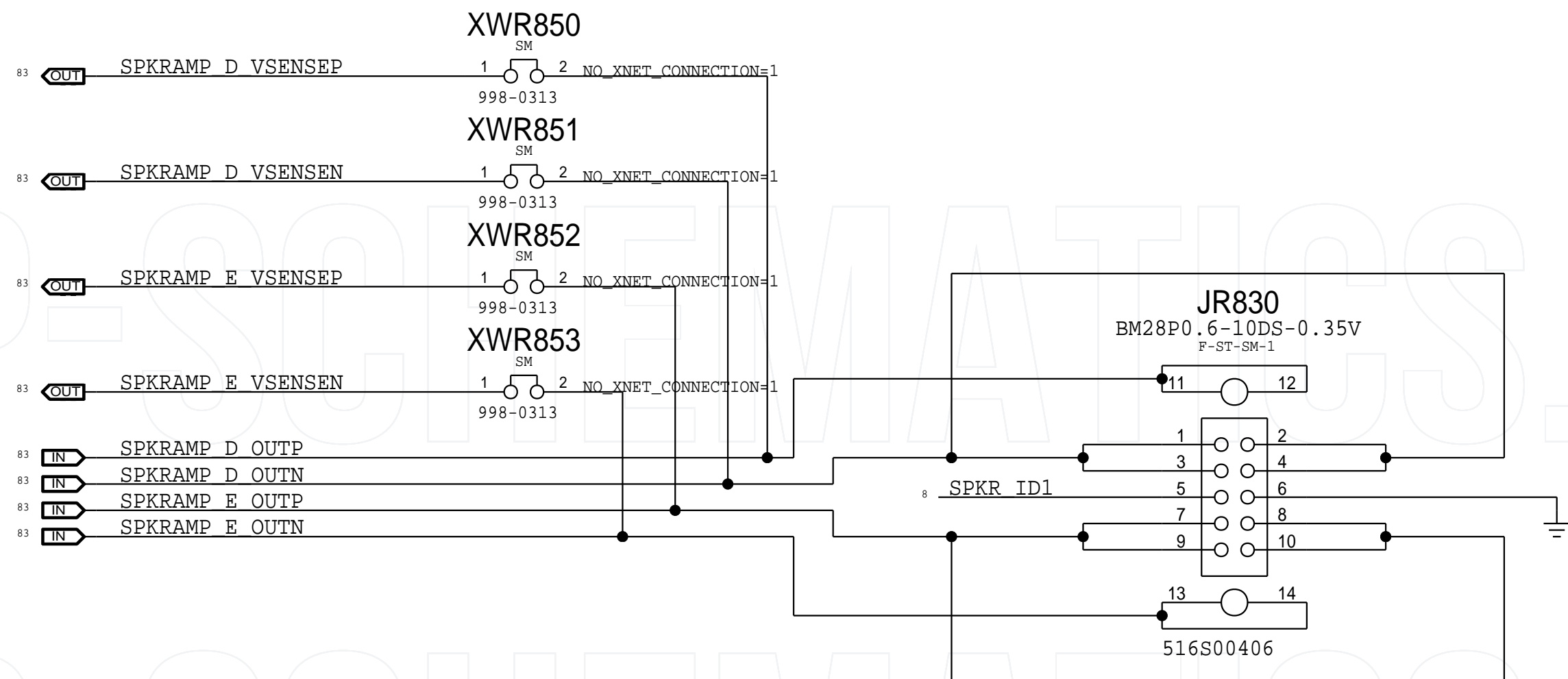


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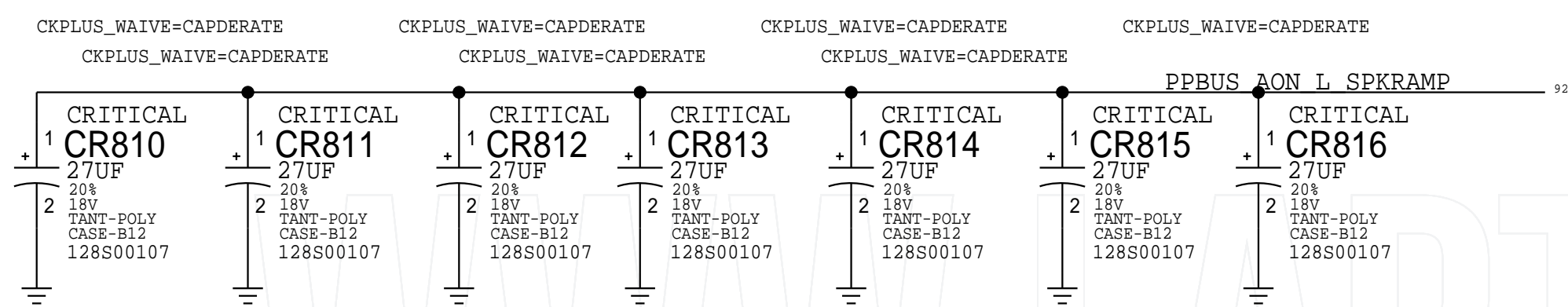
A LEFT SPEAKER CONNECTOR



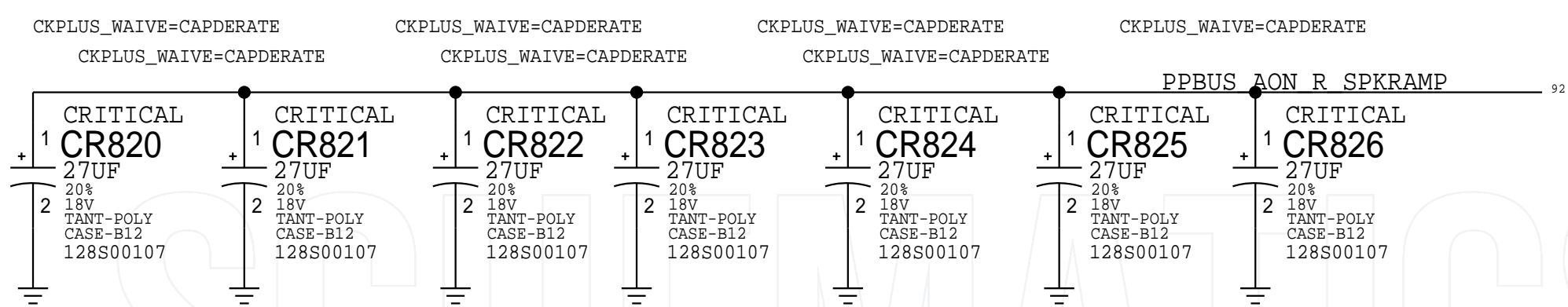
B RIGHT SPEAKER CONNECTOR



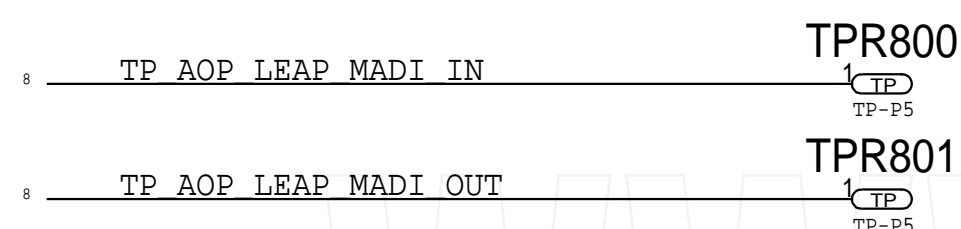
C LEFT SPEAKER AMP BULK CAP



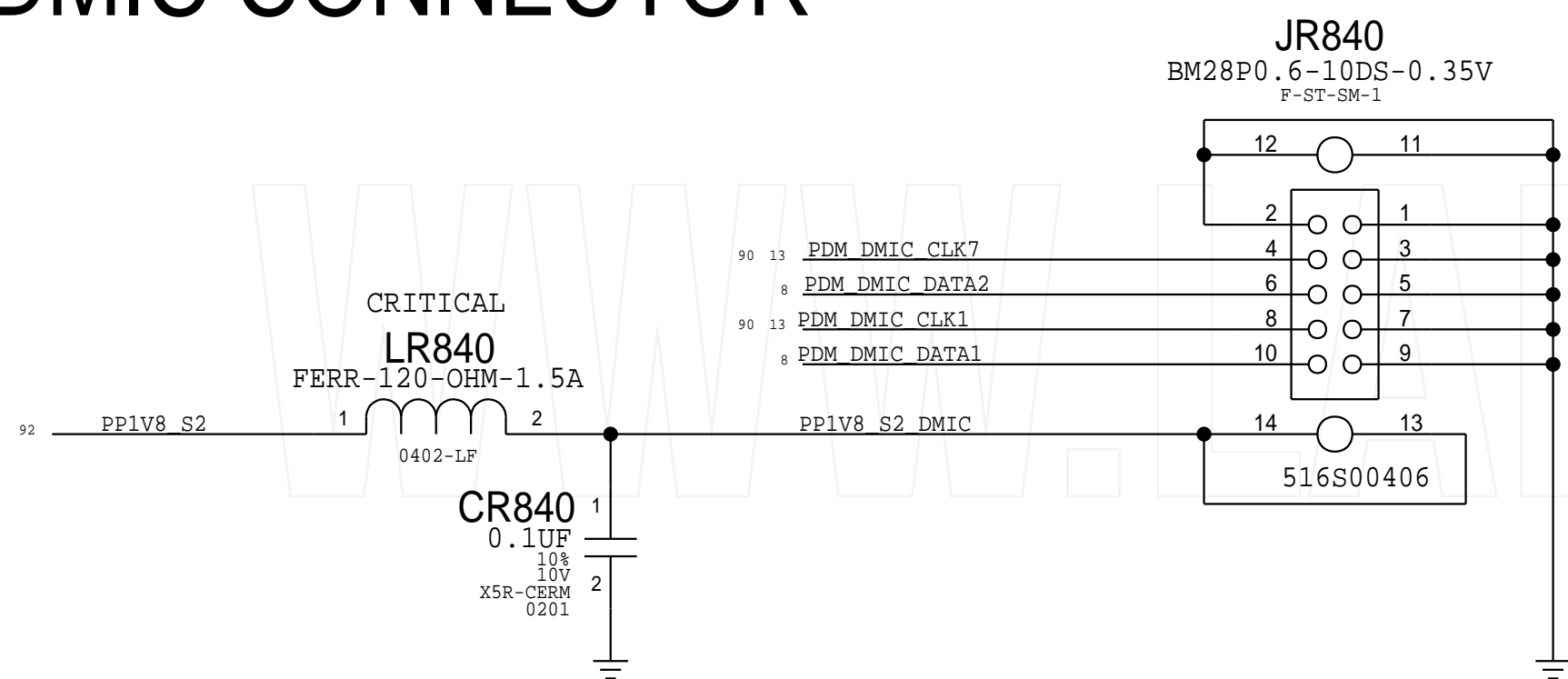
D RIGHT SPEAKER AMP BULK CAP



E MADI TEST POINT



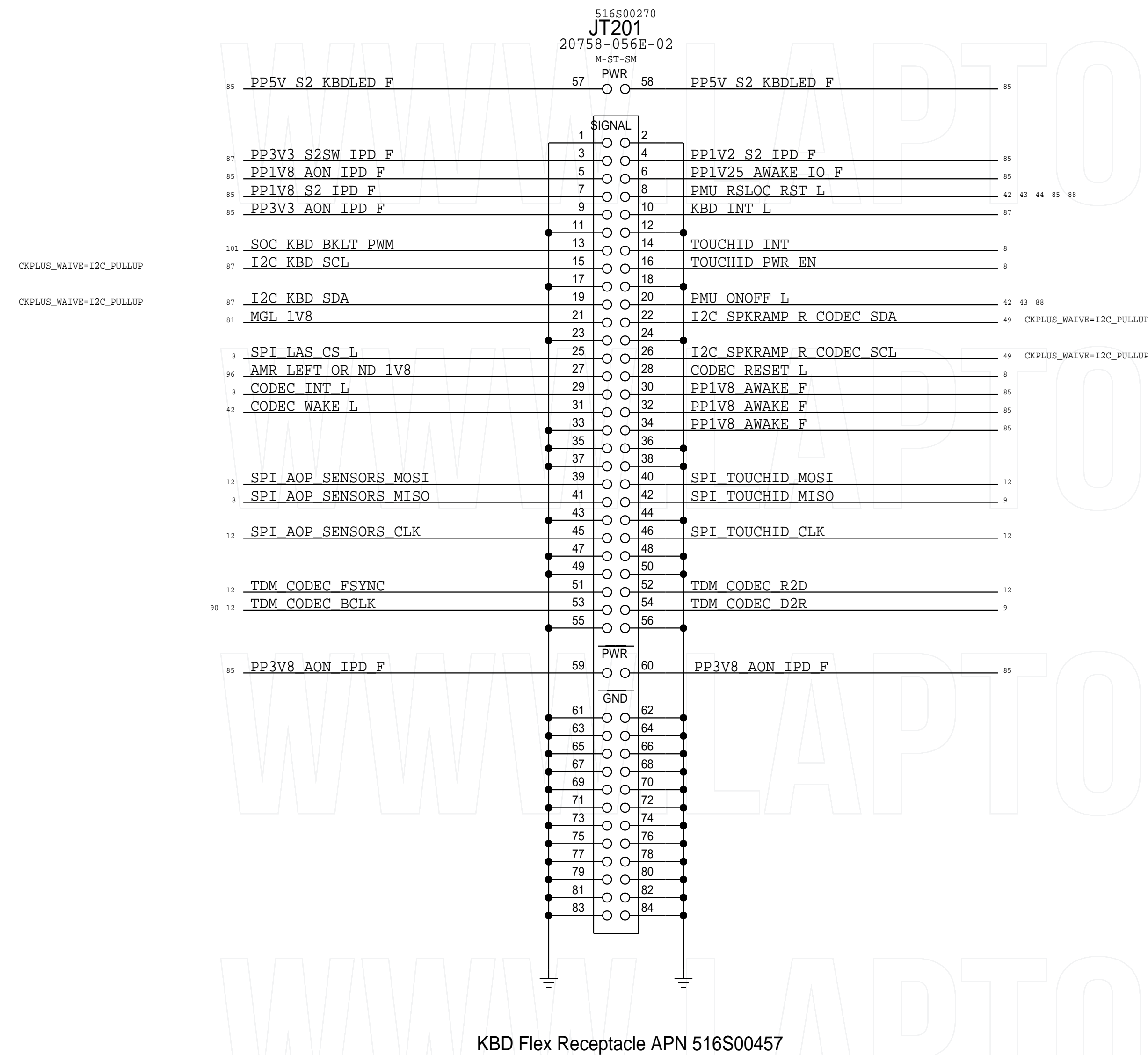
F DMIC CONNECTOR



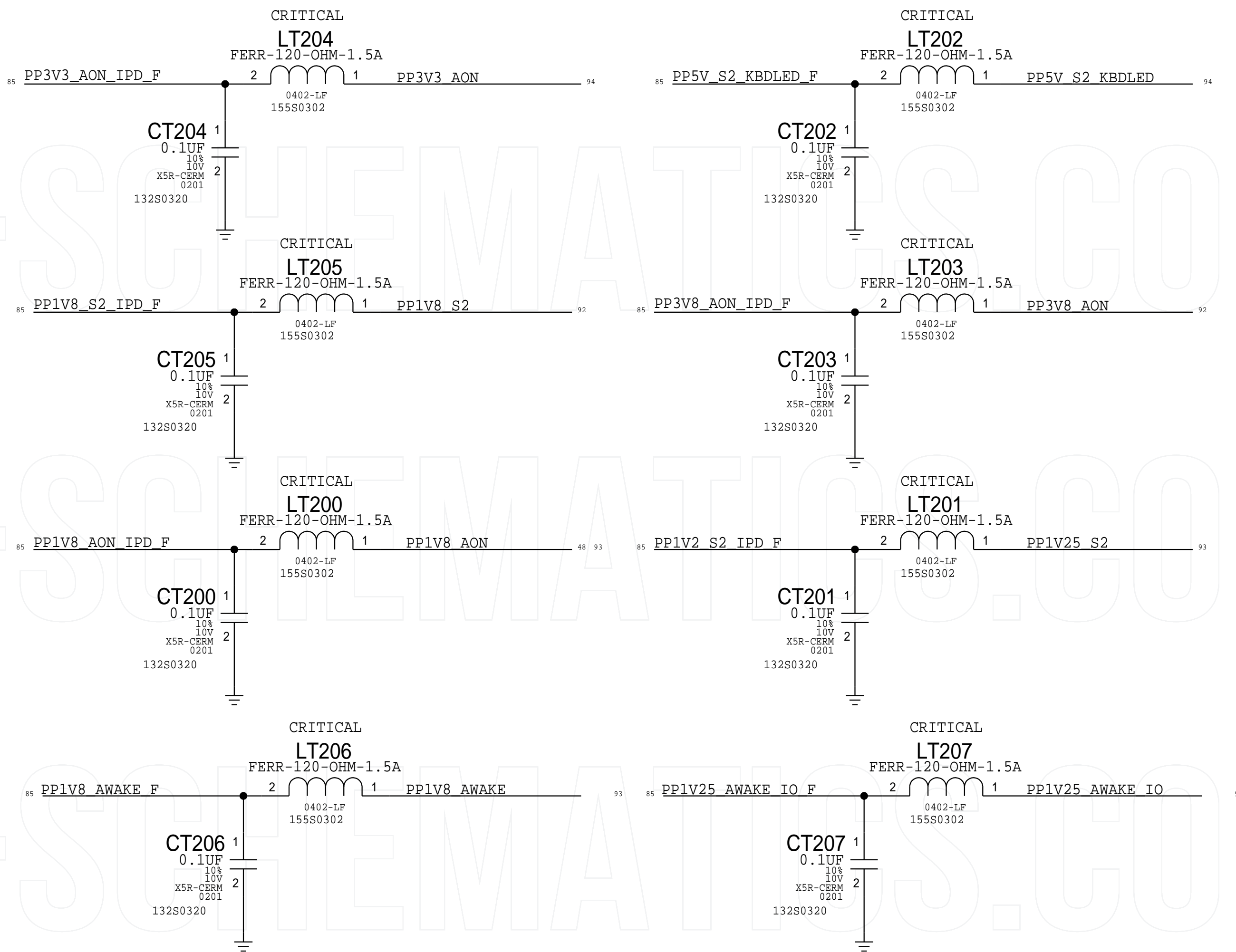
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BOM_COST_GROUP=AUDIO

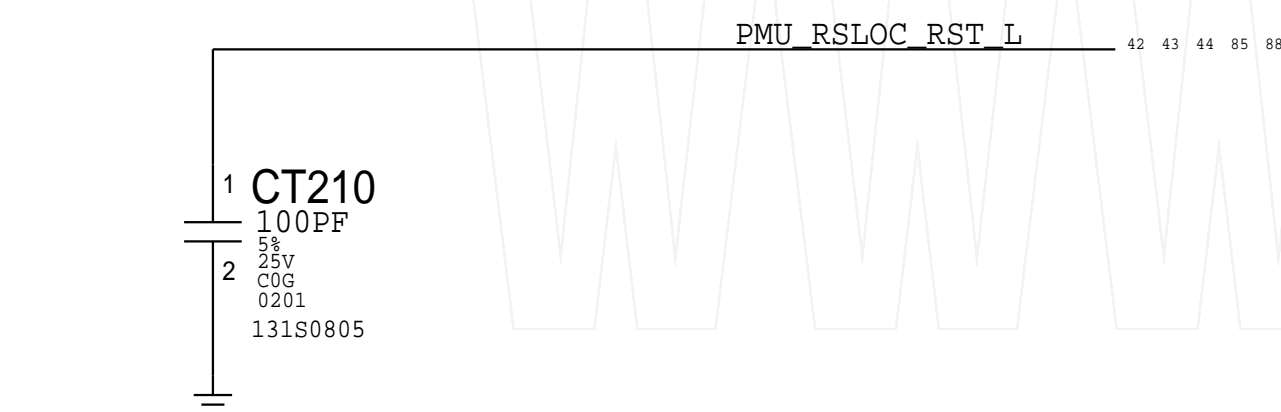
A KBD B2B CONNECTOR



B KBD PWR FILTER



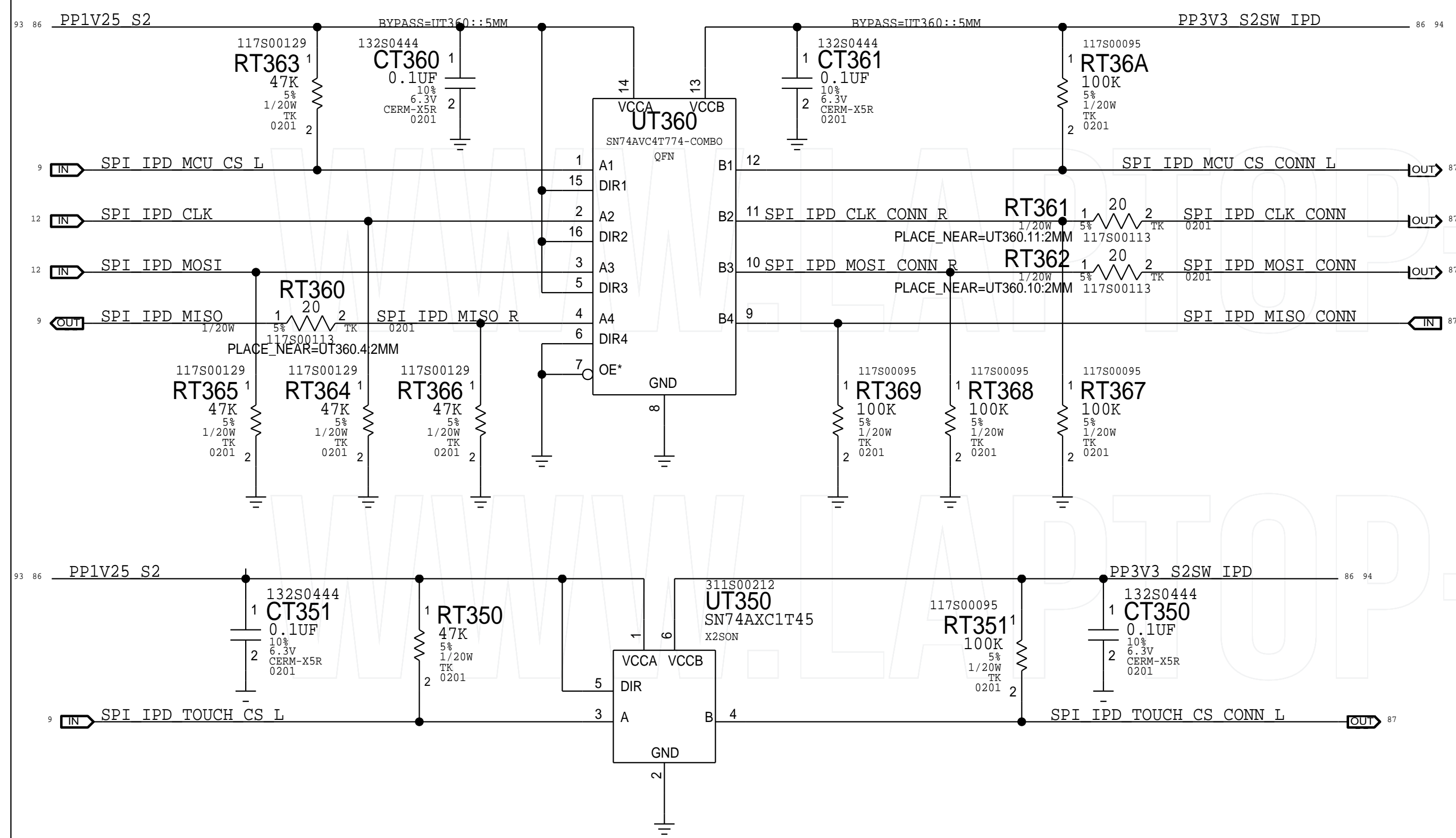
C Keyboard Control



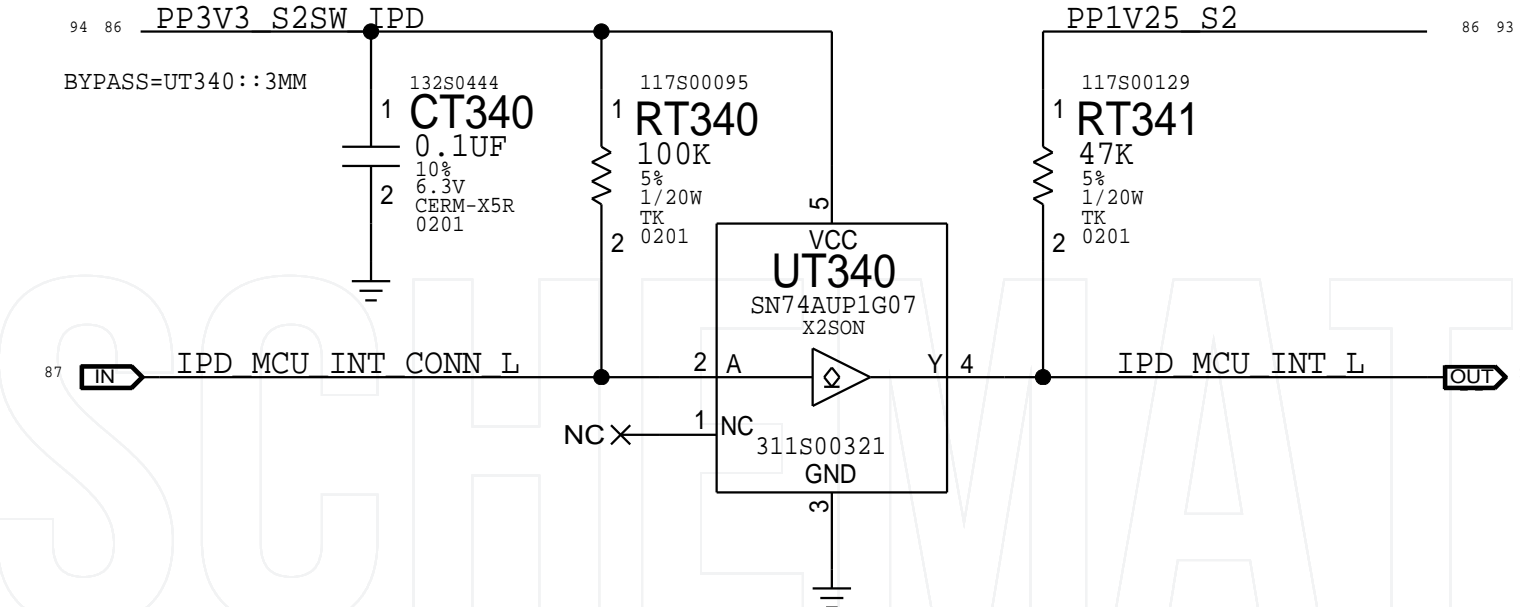
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Keyboard Connector		
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BOM_COST_GROUP=KEYBOARD

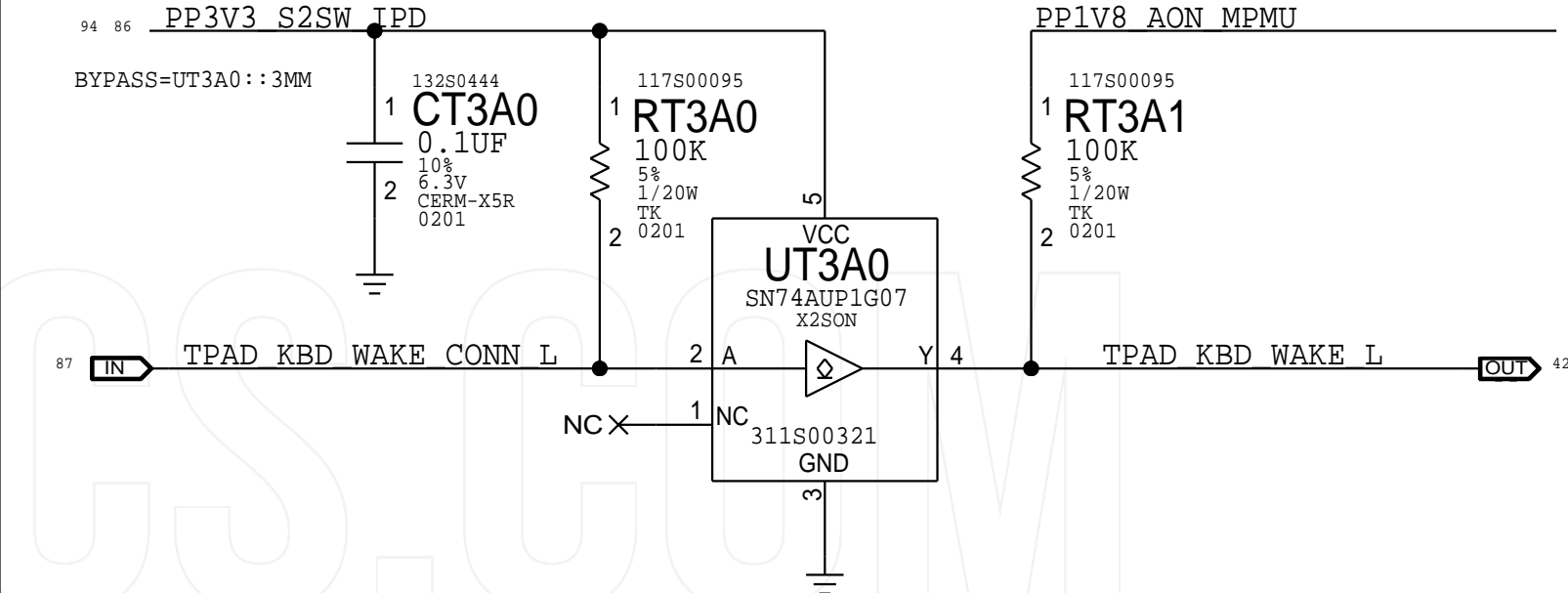
A Trackpad SPI Bus Level Shifter



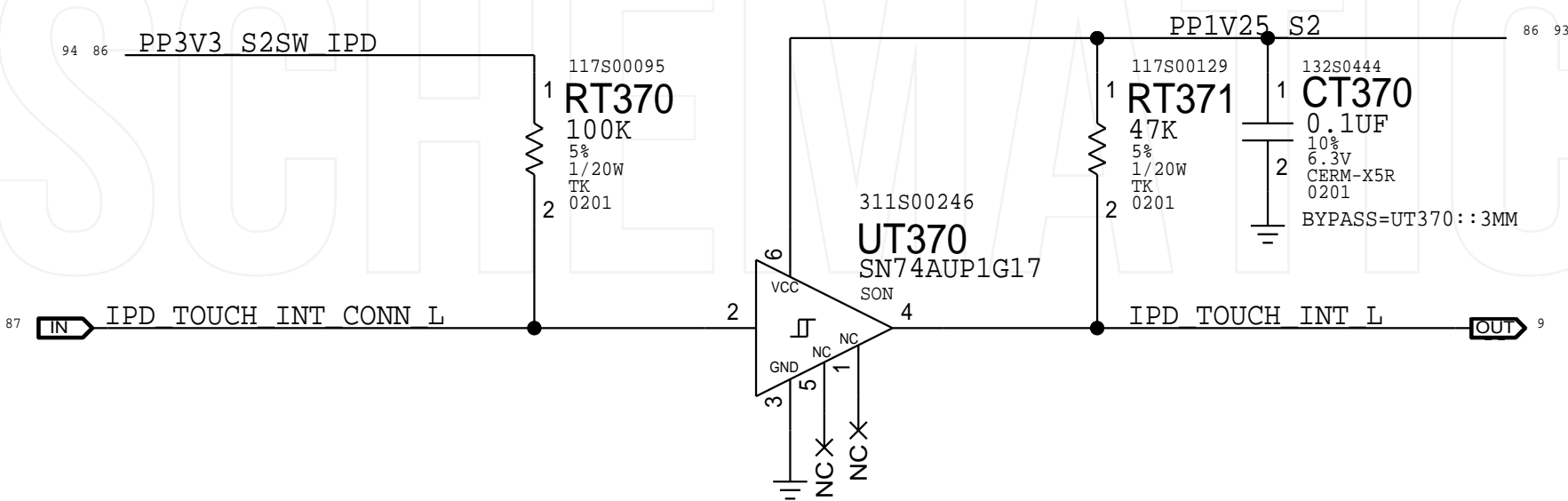
B Trackpad MCU_INT_L LS



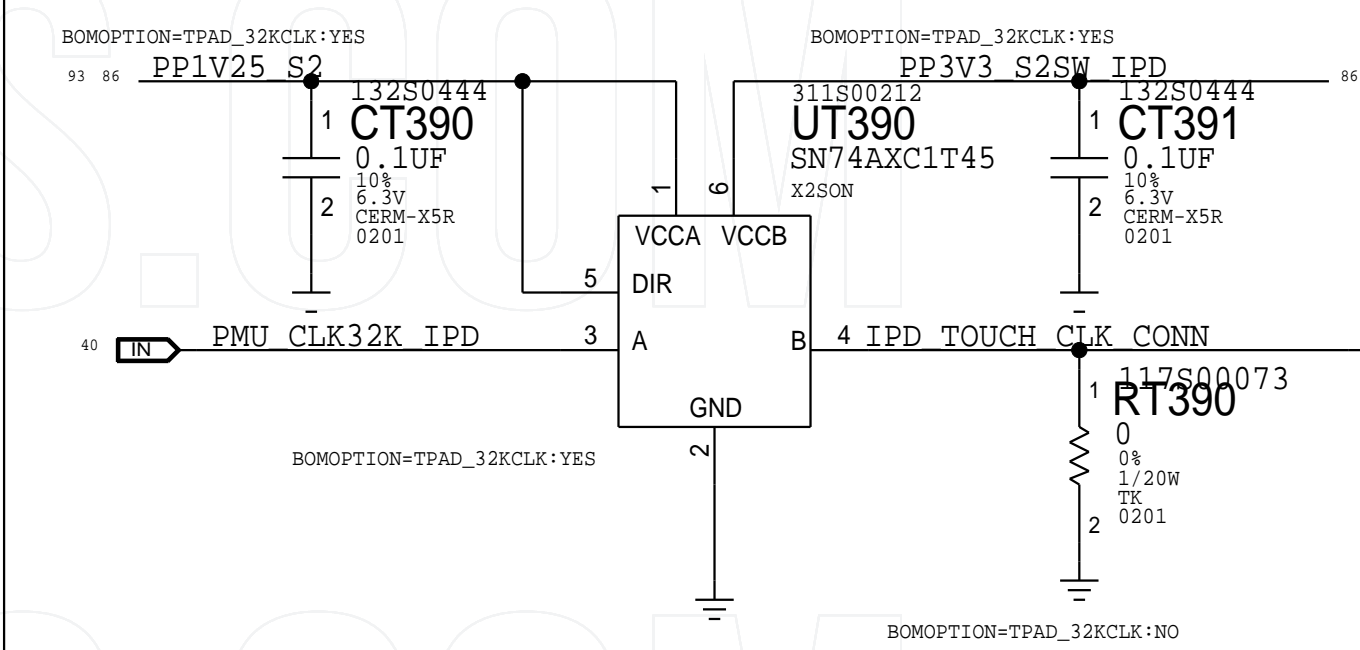
C Trackpad WAKE_L LS



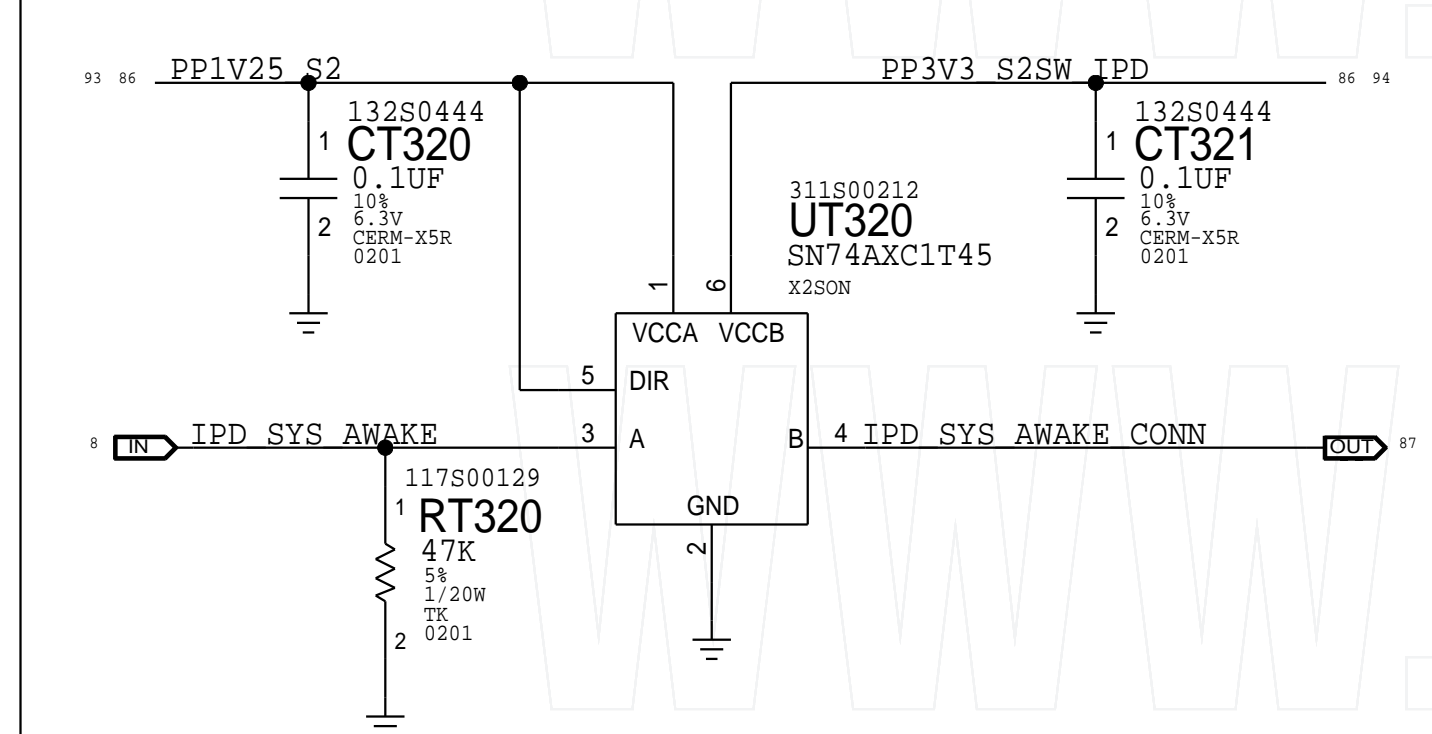
D Trackpad TOUCH_INT_L LS



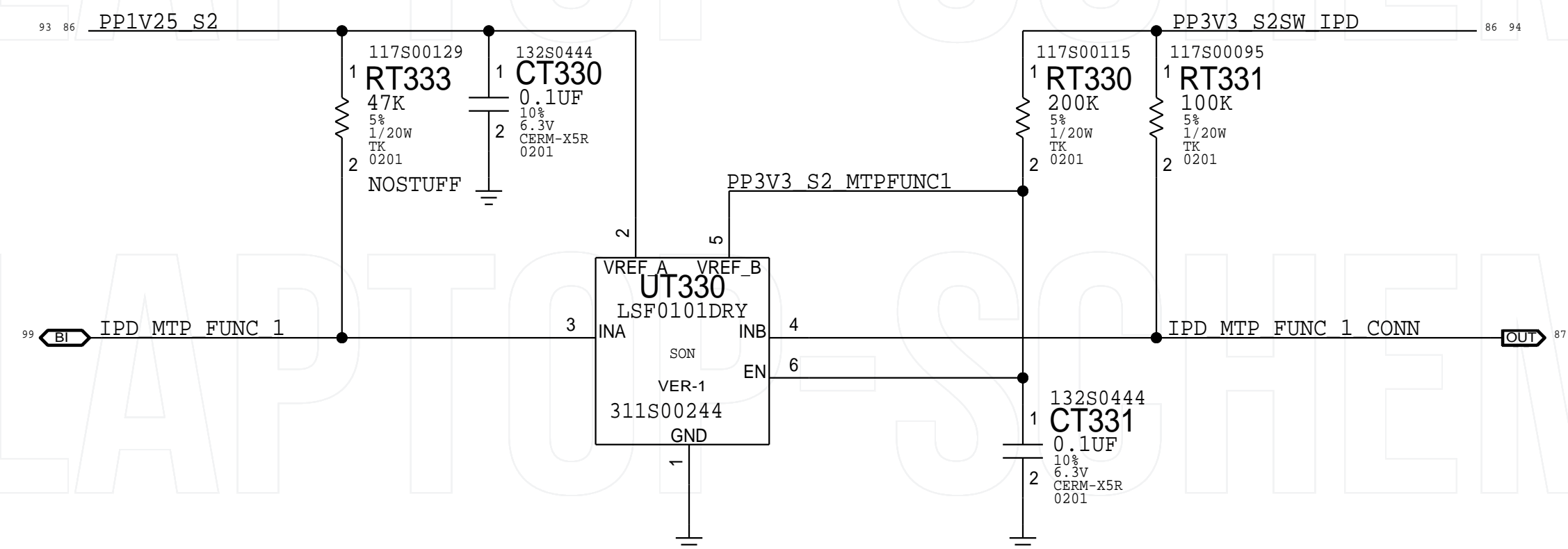
E Trackpad 32kHz Clock LS



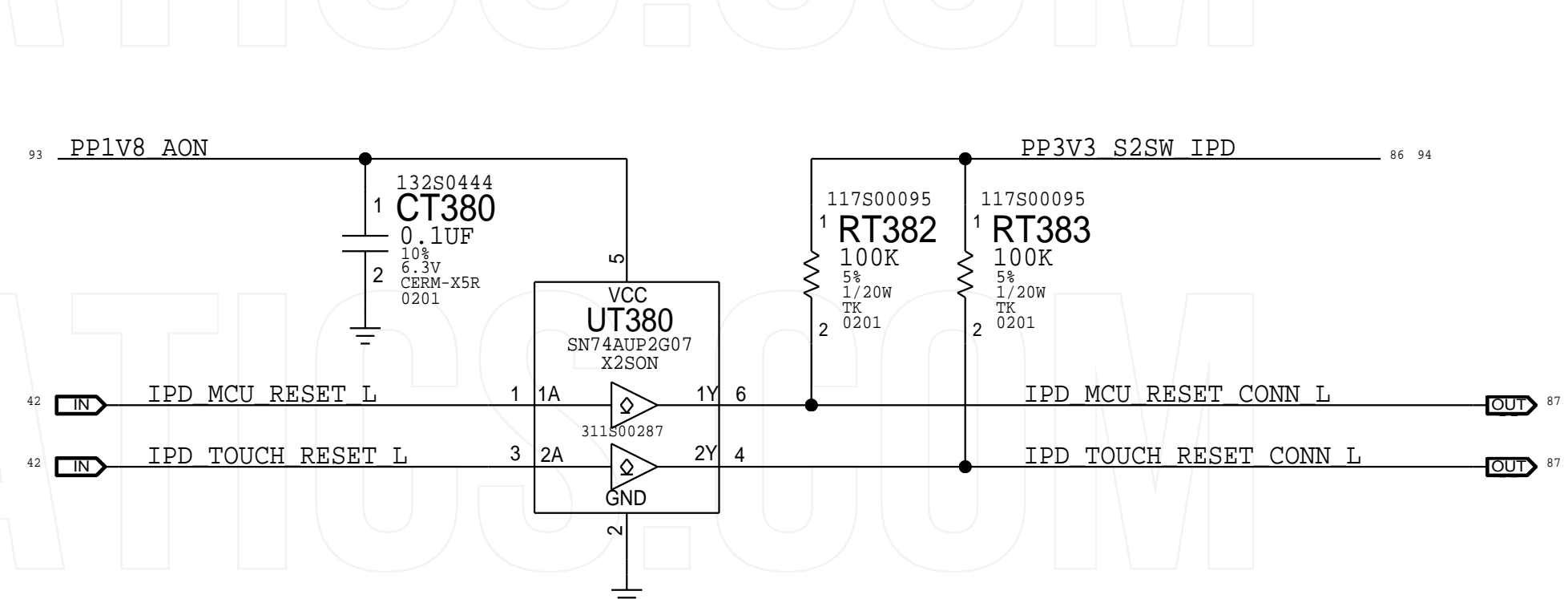
F Trackpad SYS_AWAKE LS



G Trackpad MTP_FUNC1 LS

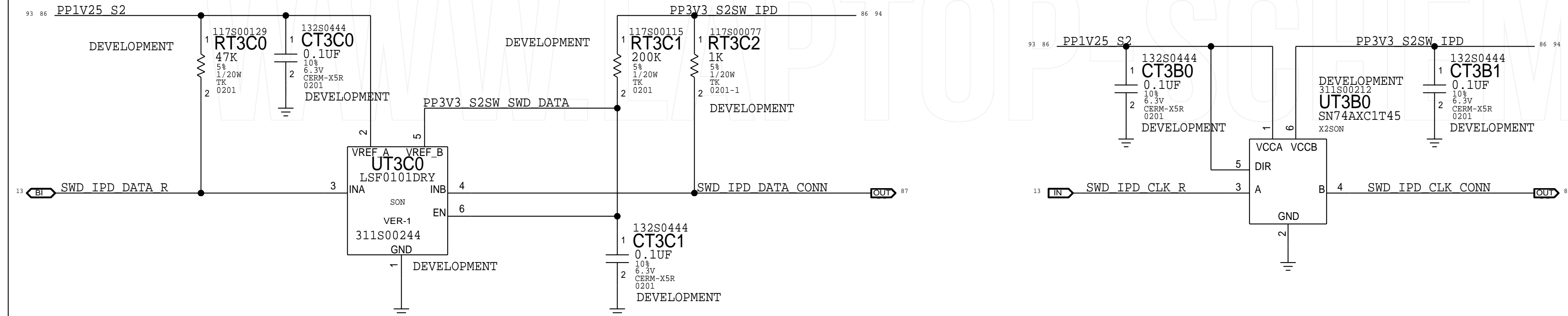


H Trackpad RESET Level Shifter



See Trackpad IPD design for RESET Pull-Up Info.

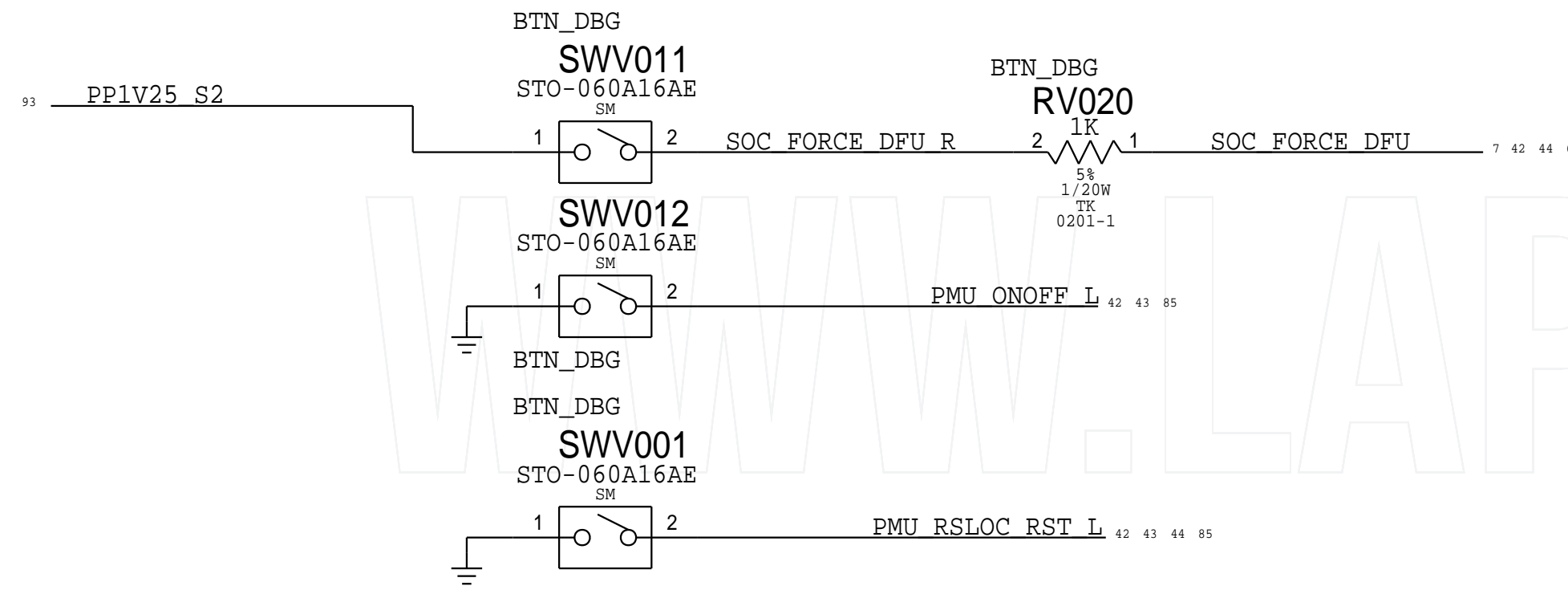
I Trackpad SWD Level Shifter



Trackpad Support		
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BOM_COST_GROUP=TRACKPAD

Ⓐ Debug Push-Buttons



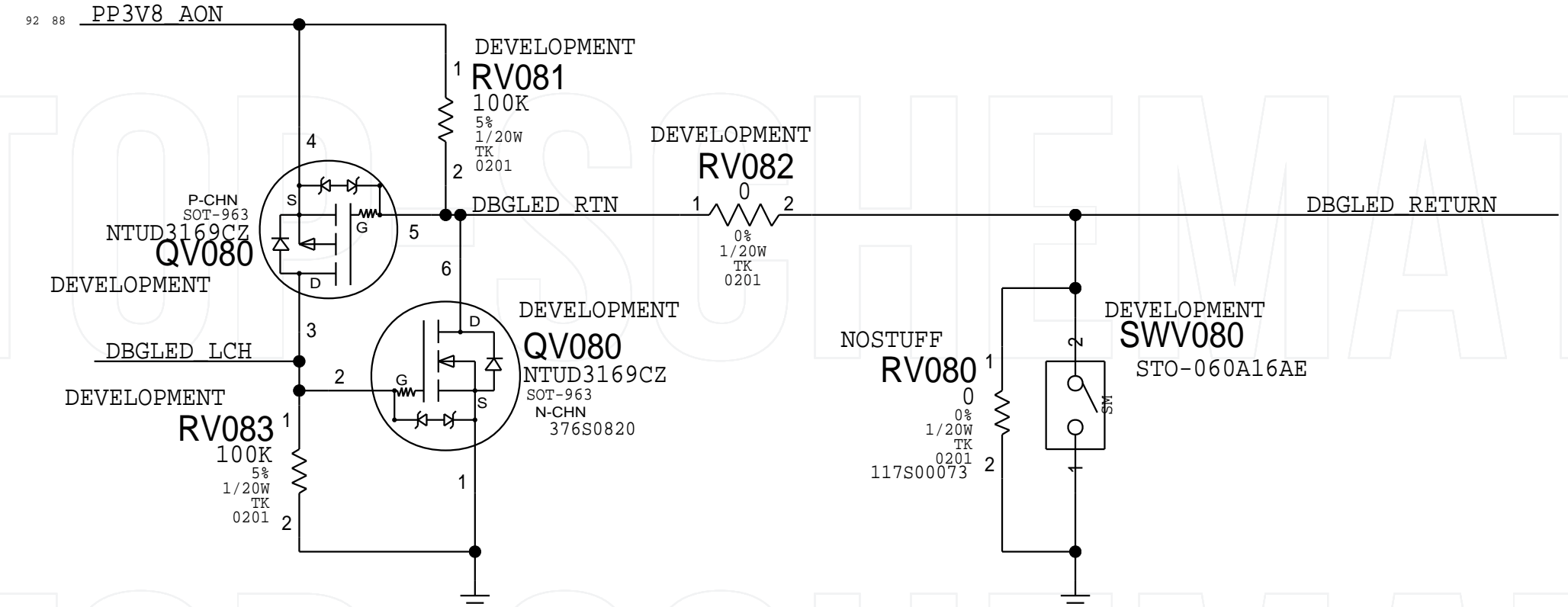
Ⓑ Debug LED Control

Debug LED Latch

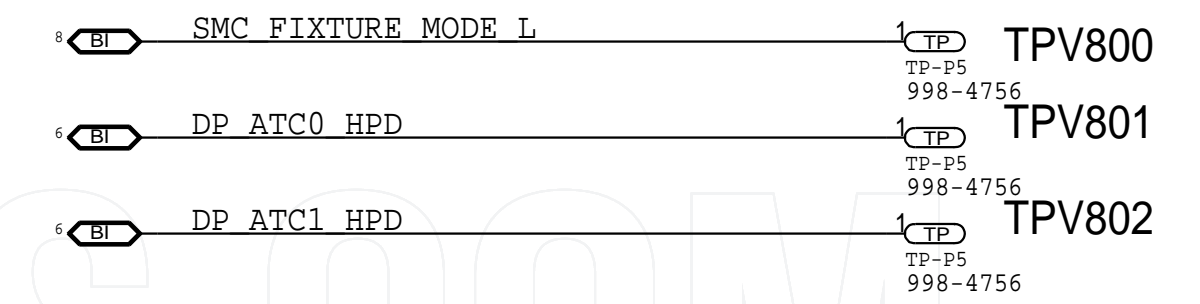
Press button once to engage.

Remove power to disengage.

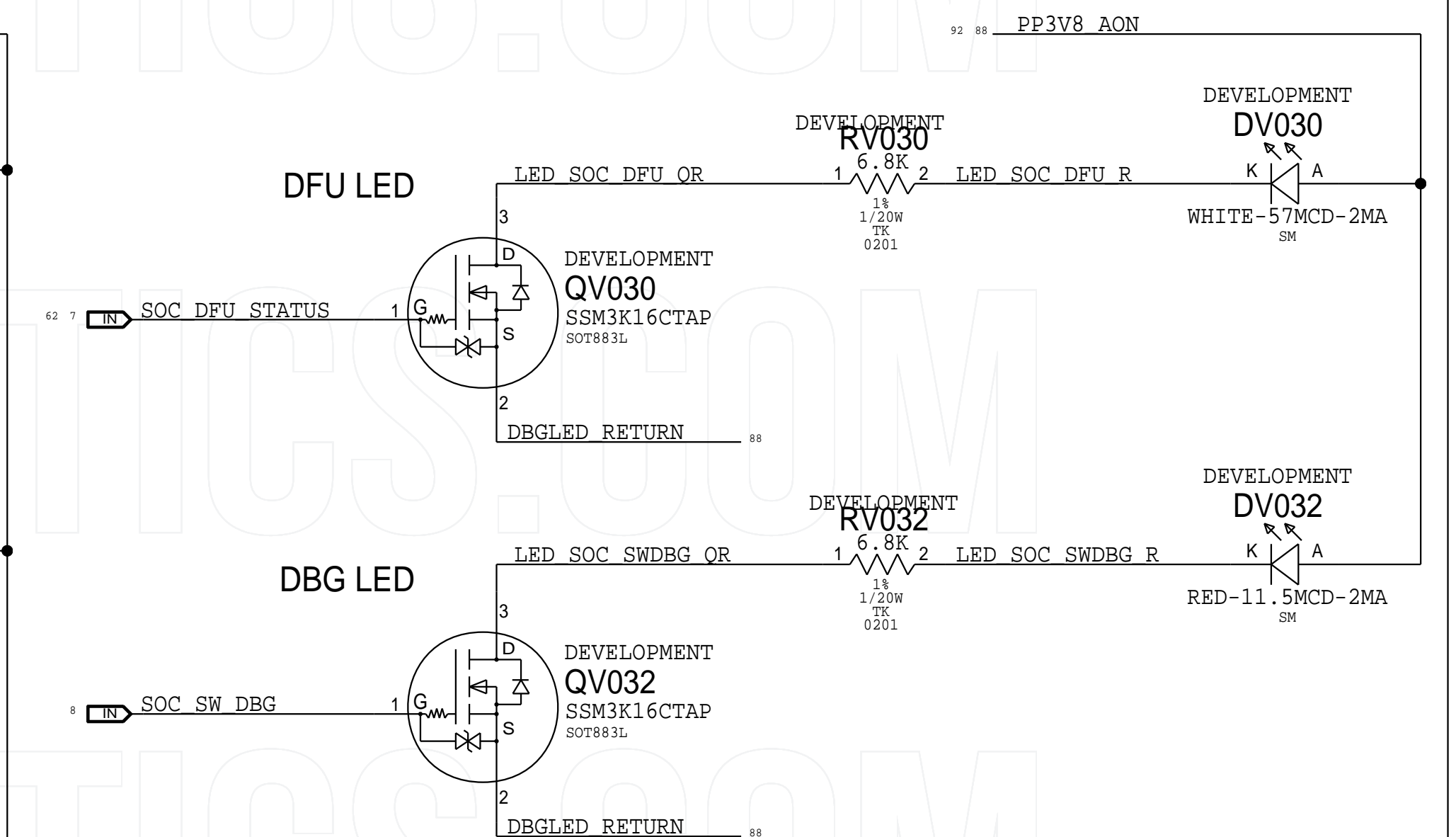
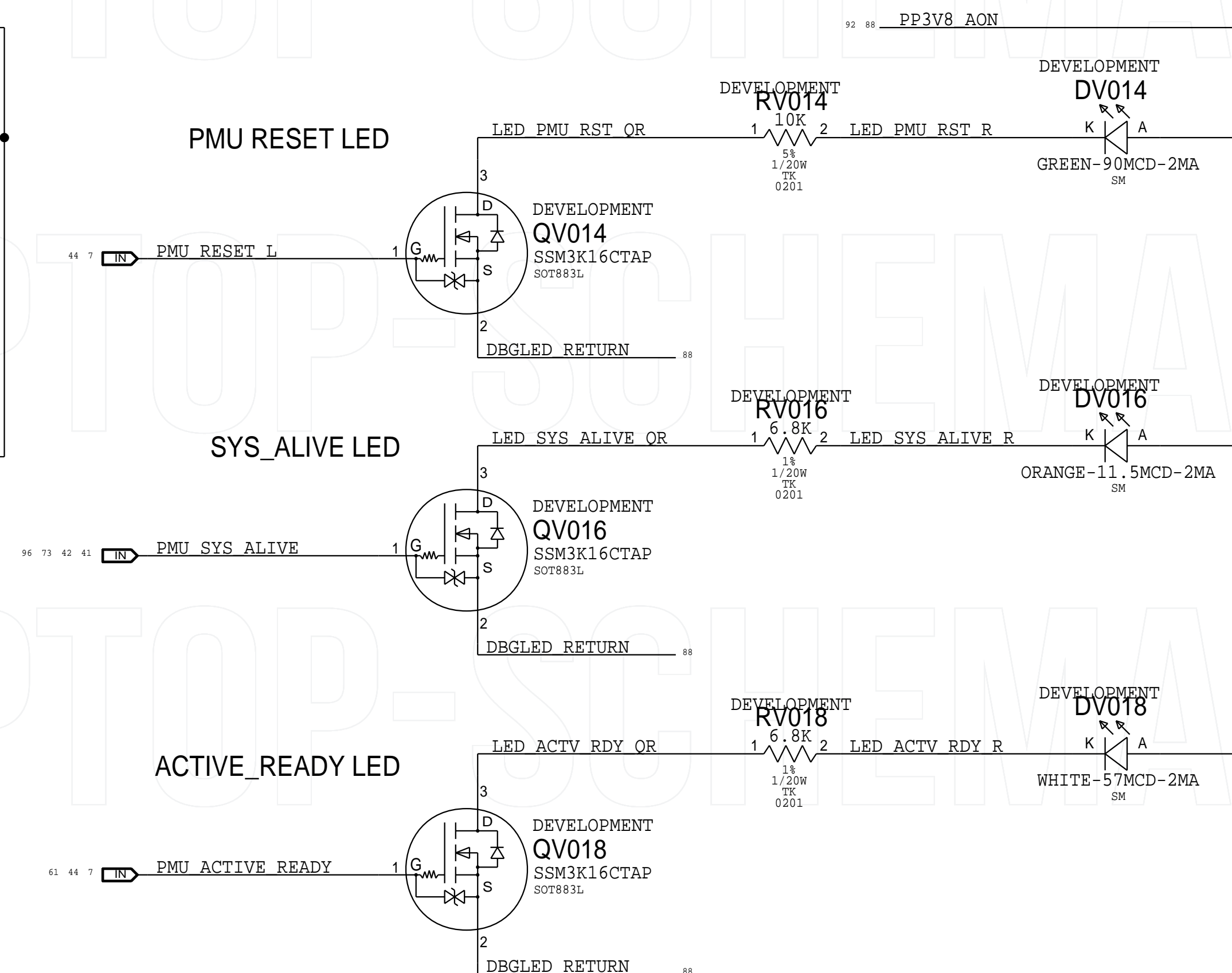
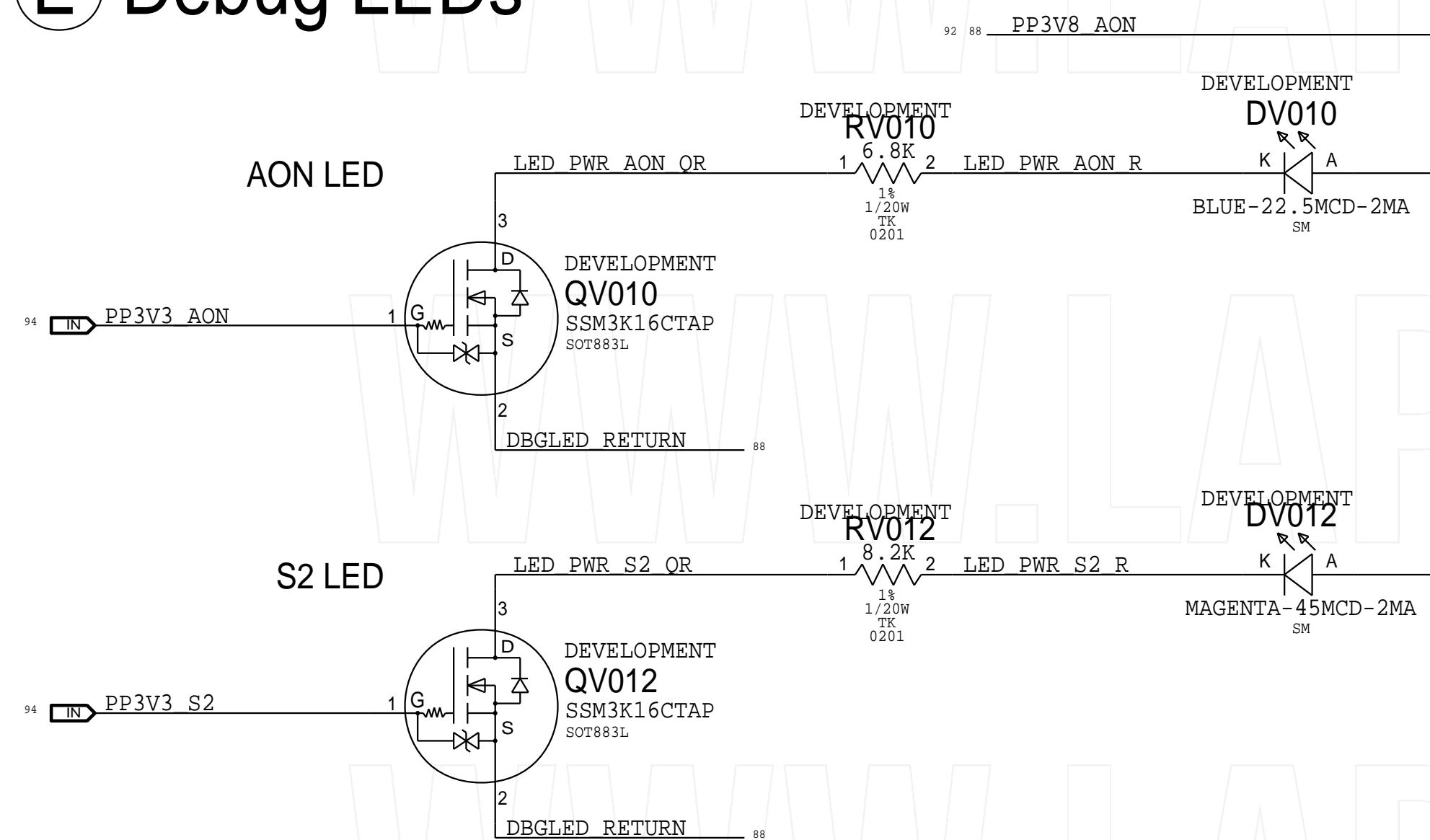
Debug LED Enable




④ Debug Test Points

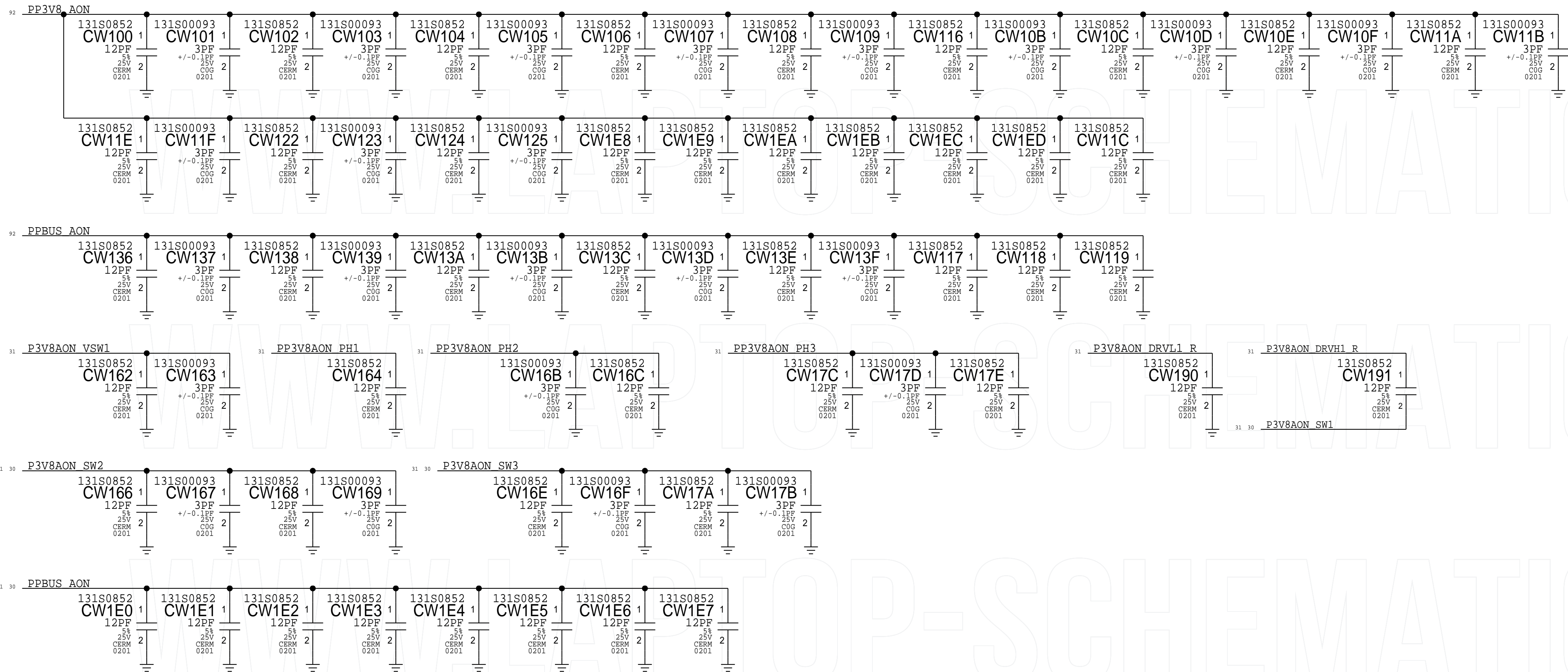


Ⓔ Debug LEDs

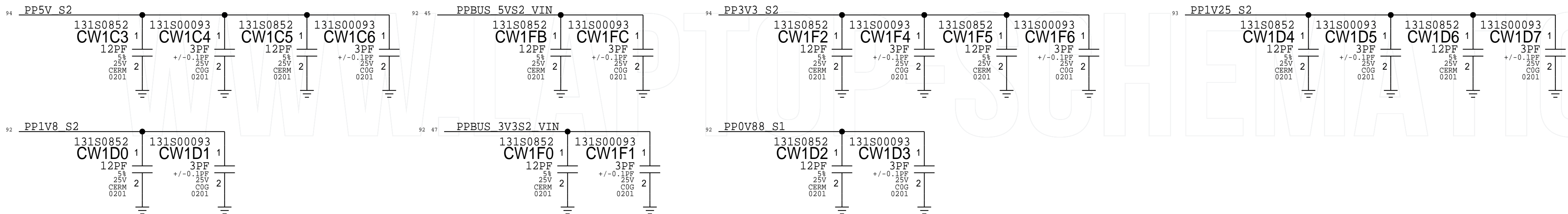



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A ICEMAN Desense



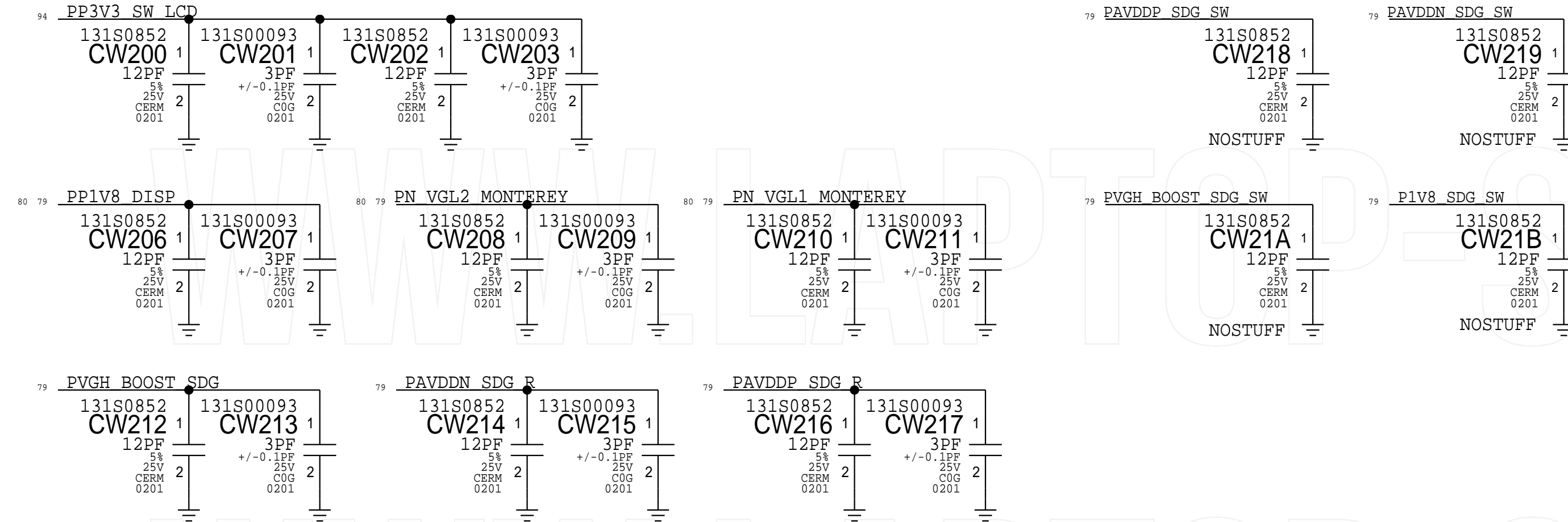
B BUCK POWER Desense



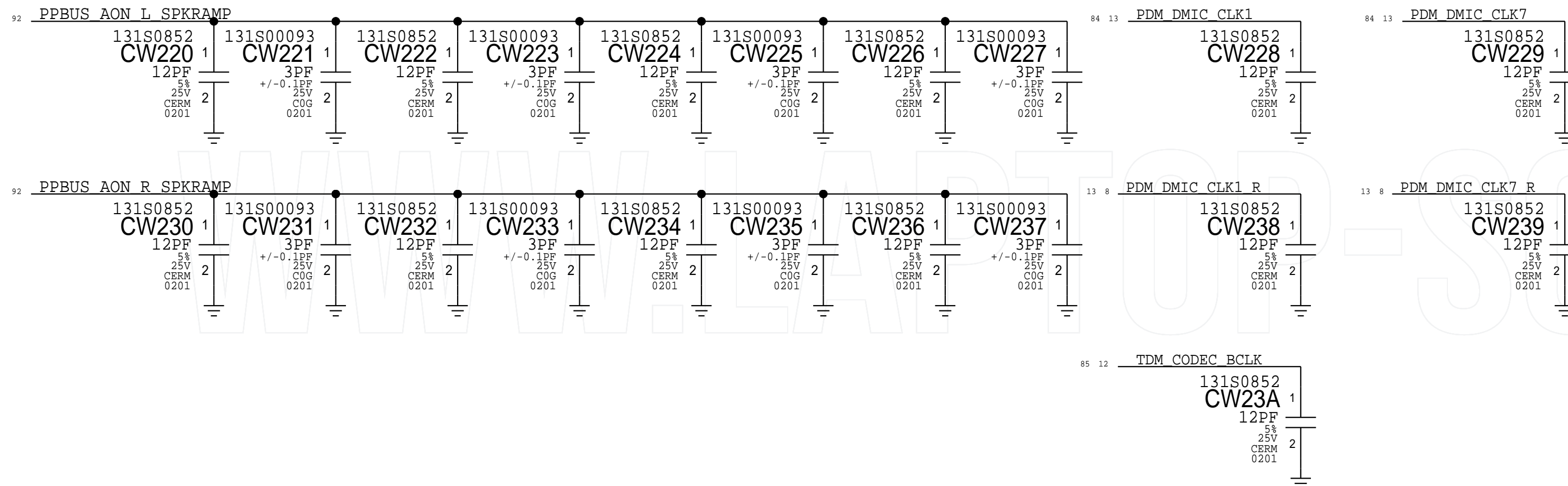
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BOM_COST_GROUP=DESENSE

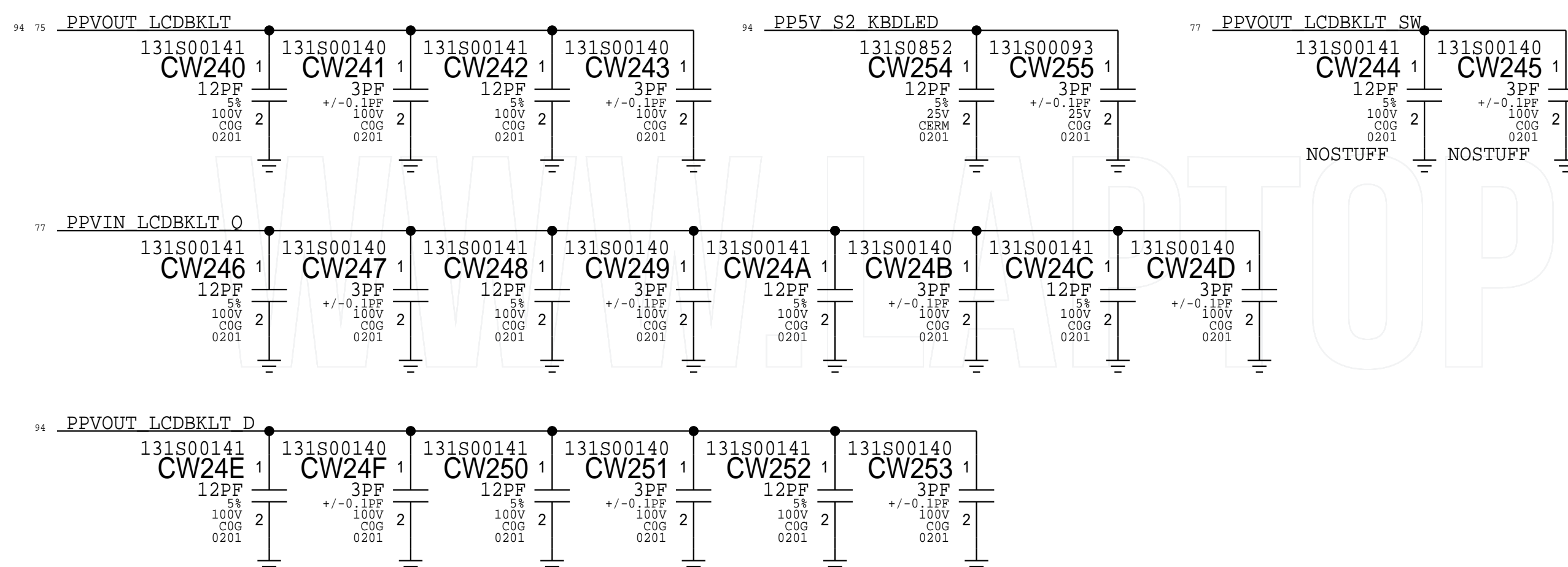
Ⓐ Display PMIC Desense



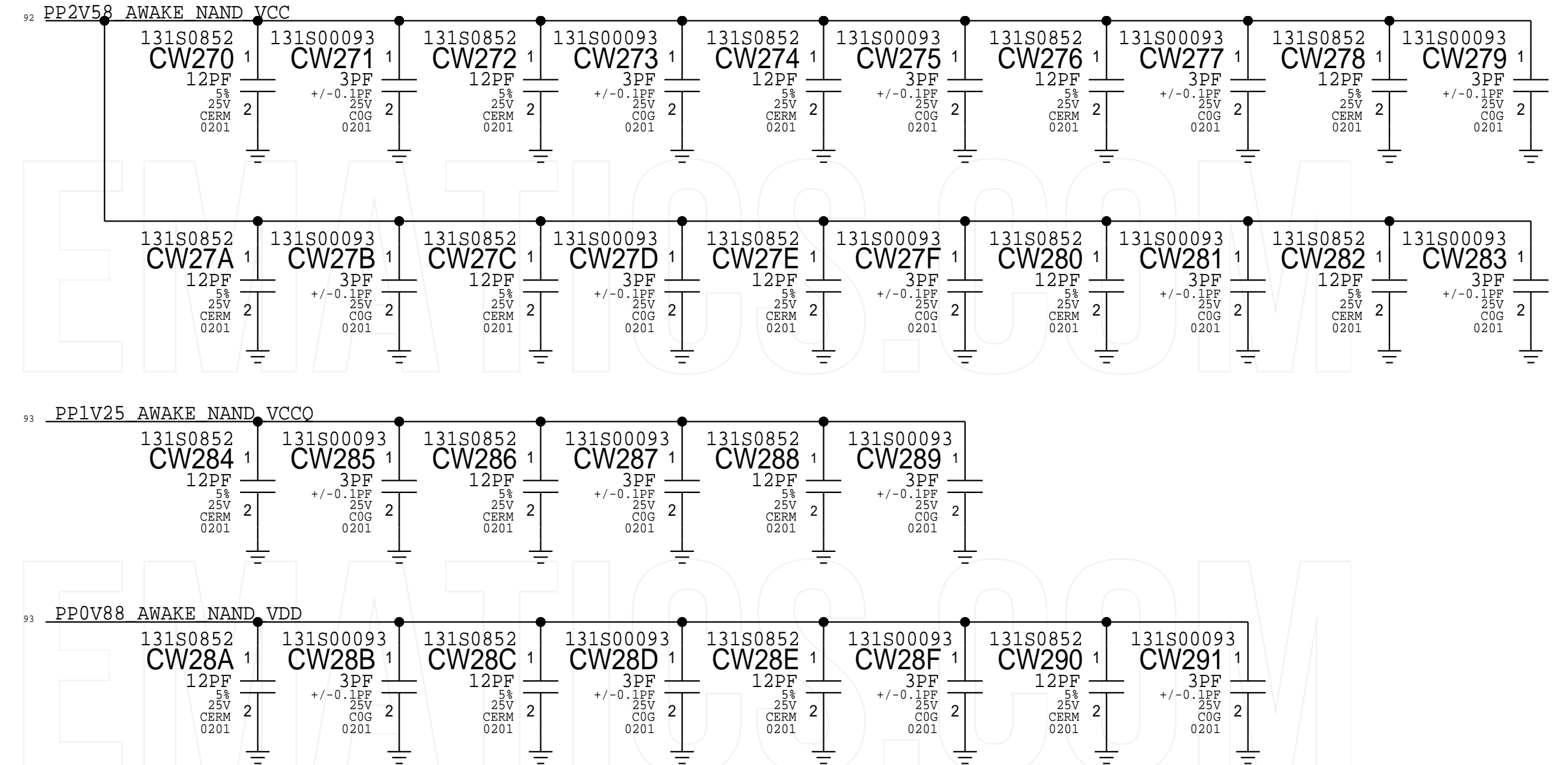
B Audio Desense



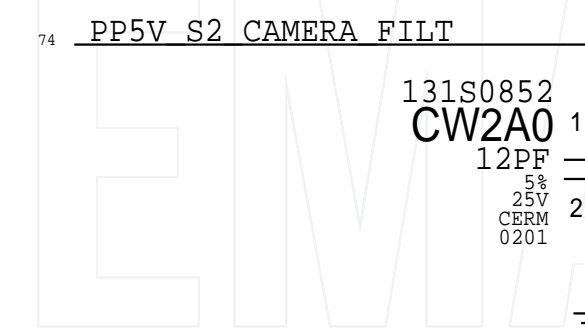
③ Display and Keyboard Backlight Desense



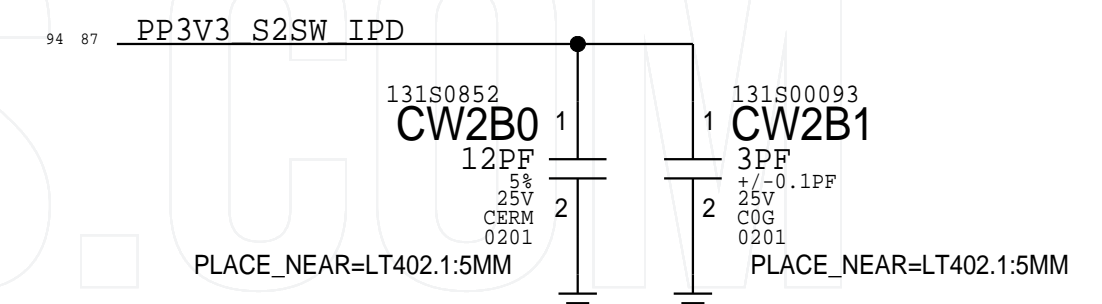
D NAND Desense



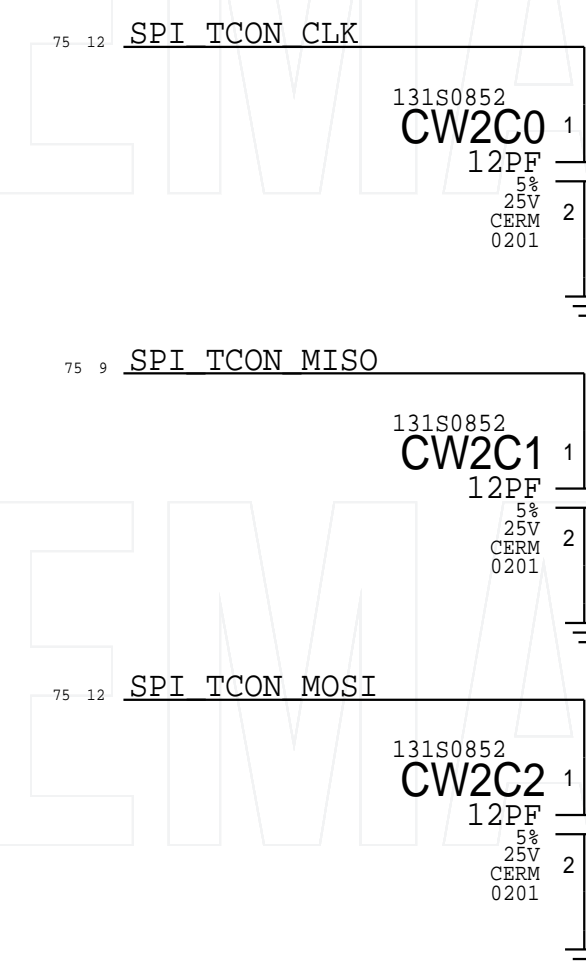
Ⓔ Camera Desense




Ⓣ Trackpad Desense

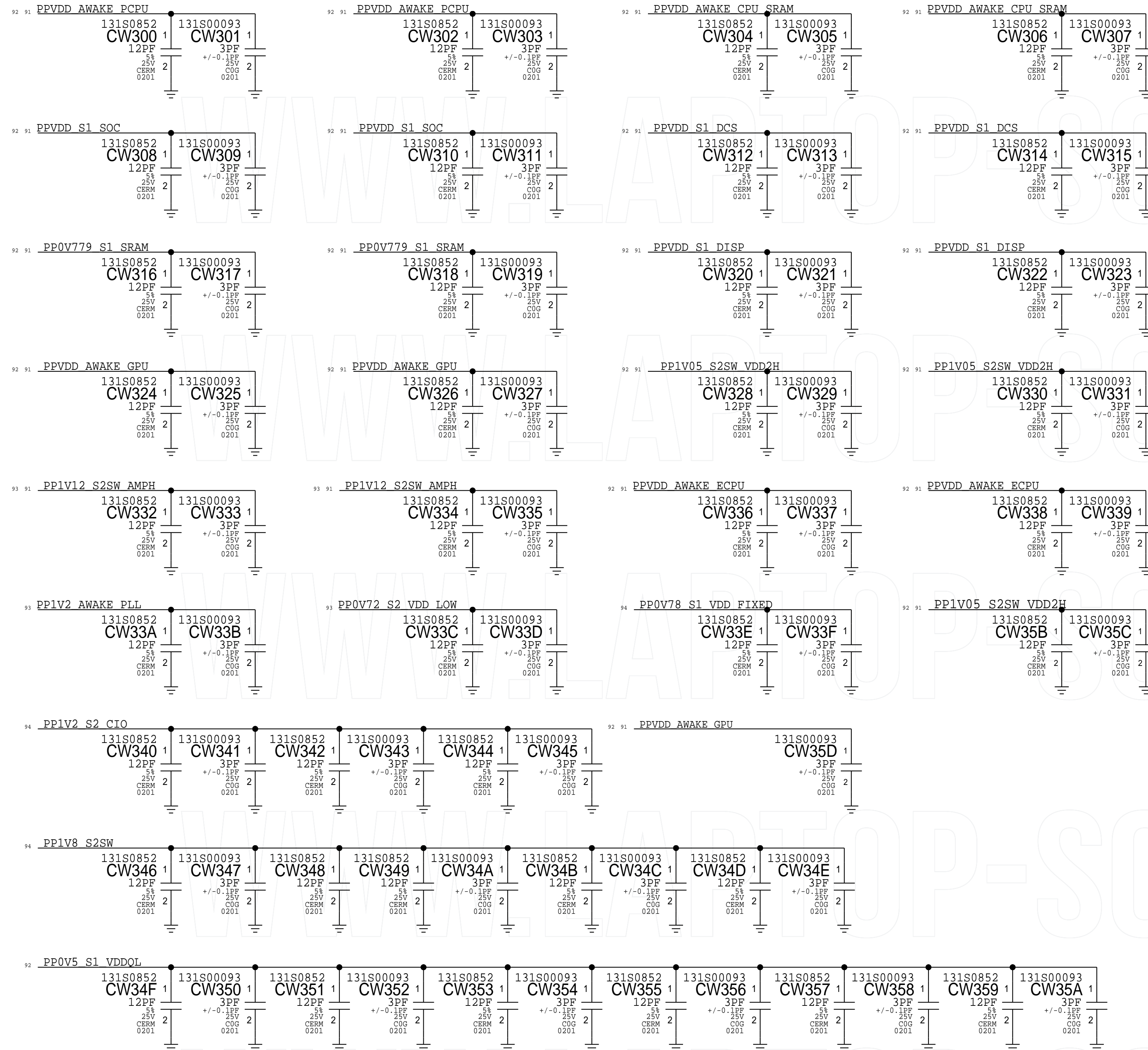



⑨ Display TCON Desense

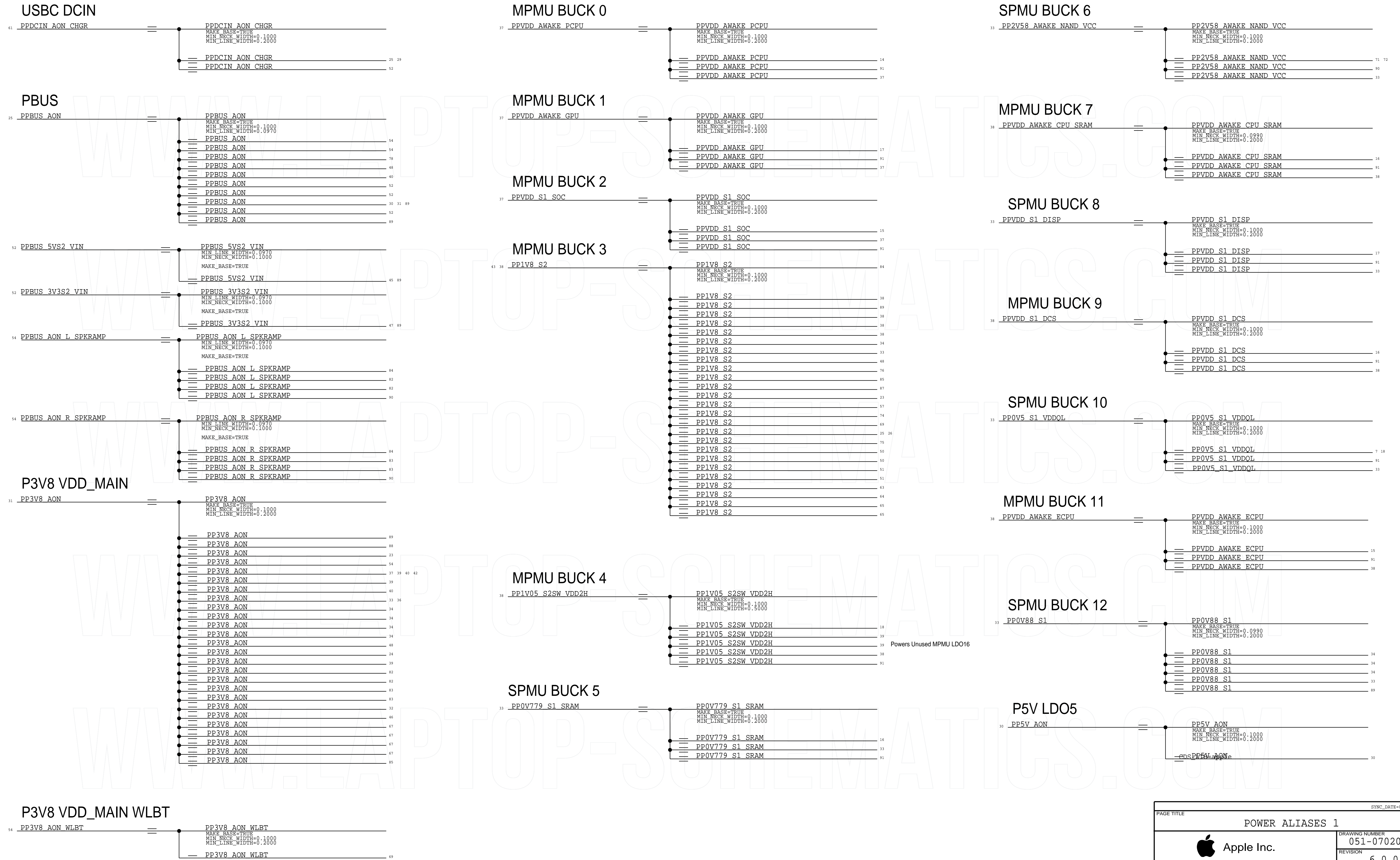


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A SOC Desense



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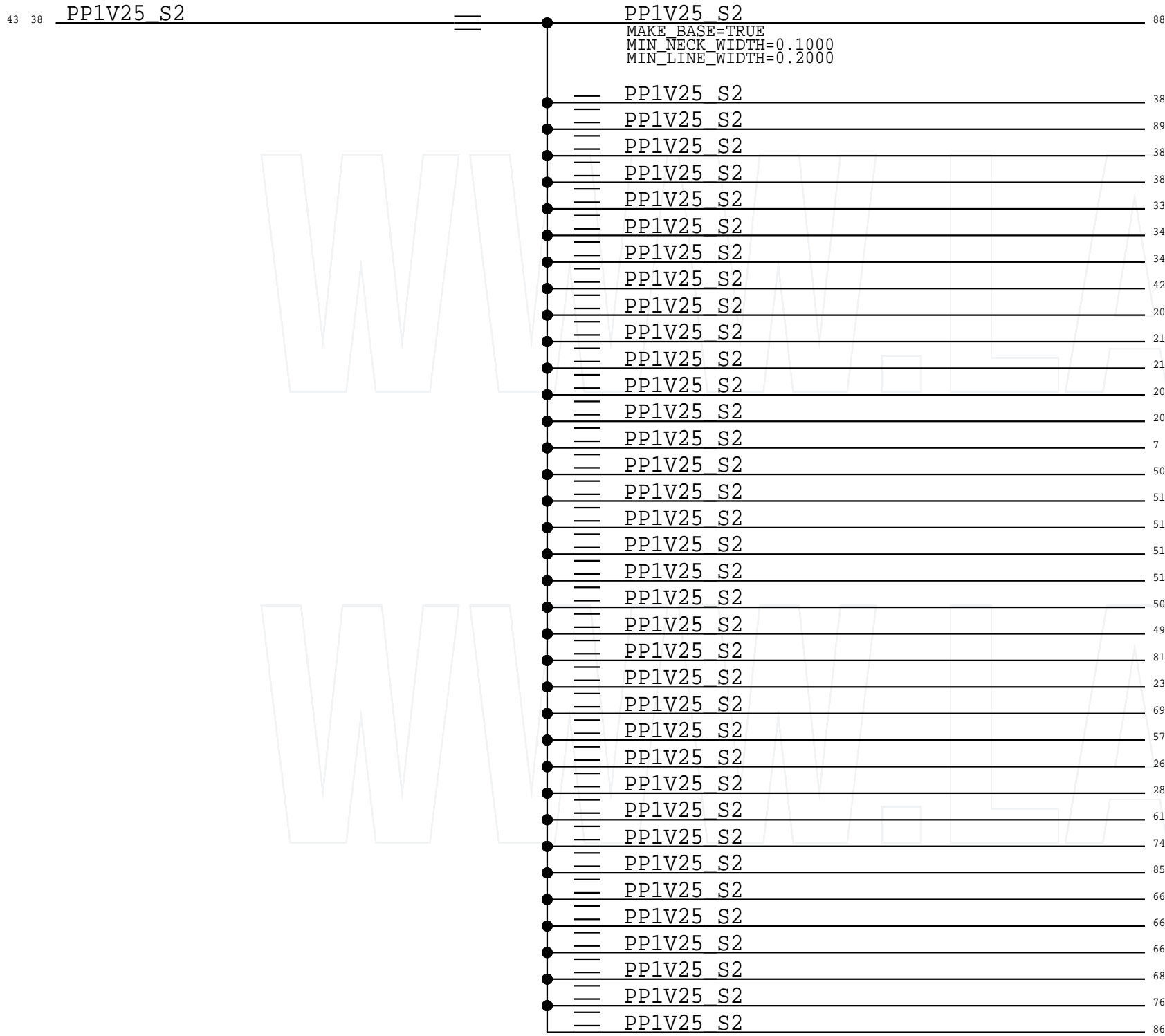
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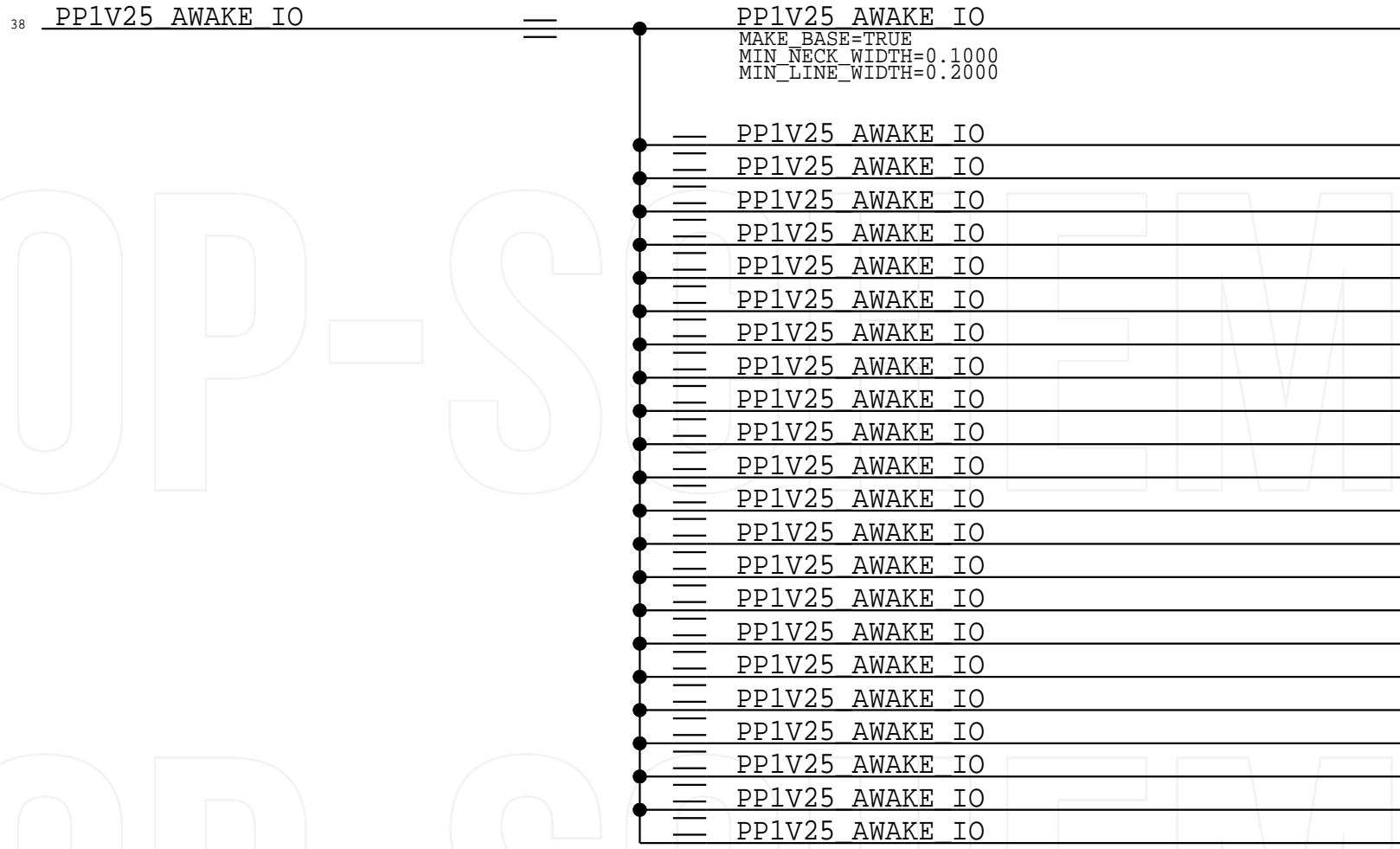
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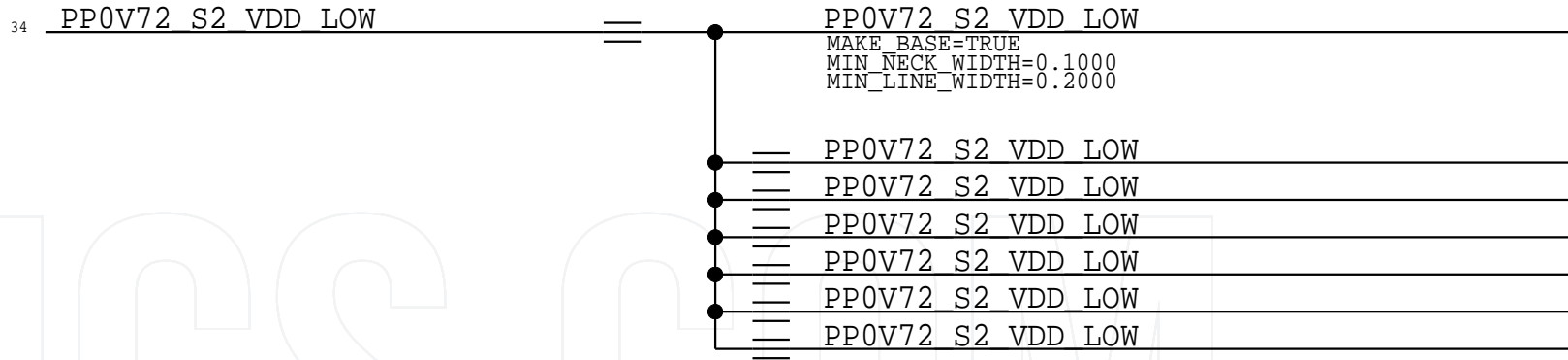
MPMU BUCK 13



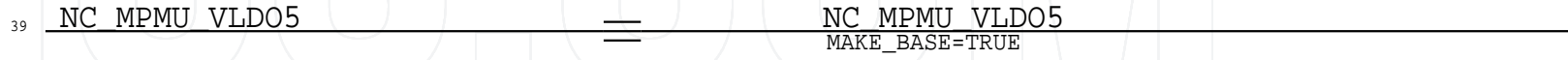
MPMU BUCK 13 SW 3



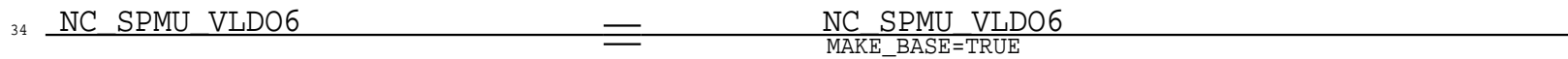
SPMU LDO 4



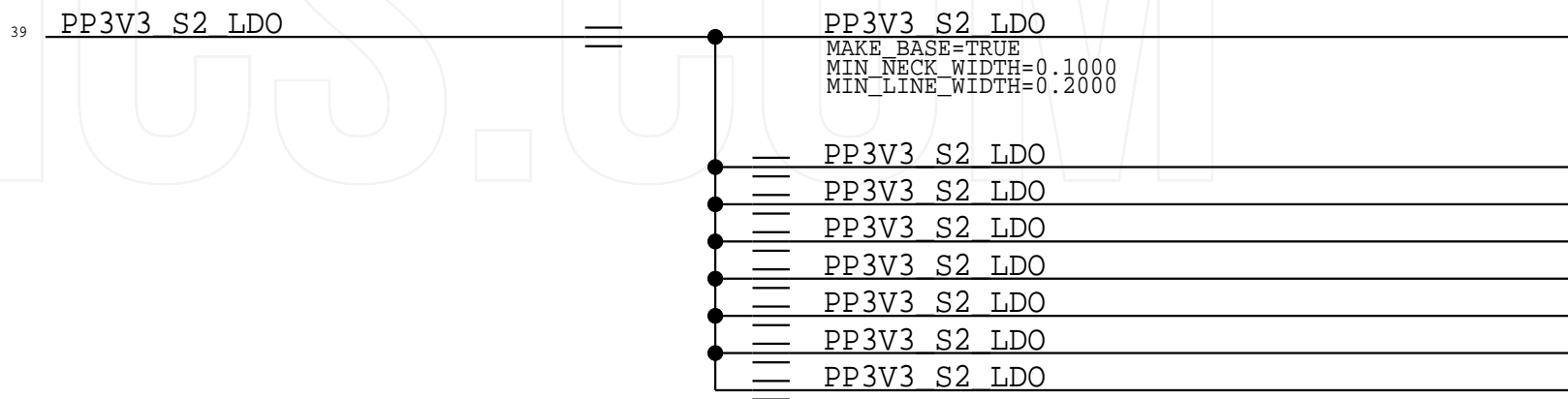
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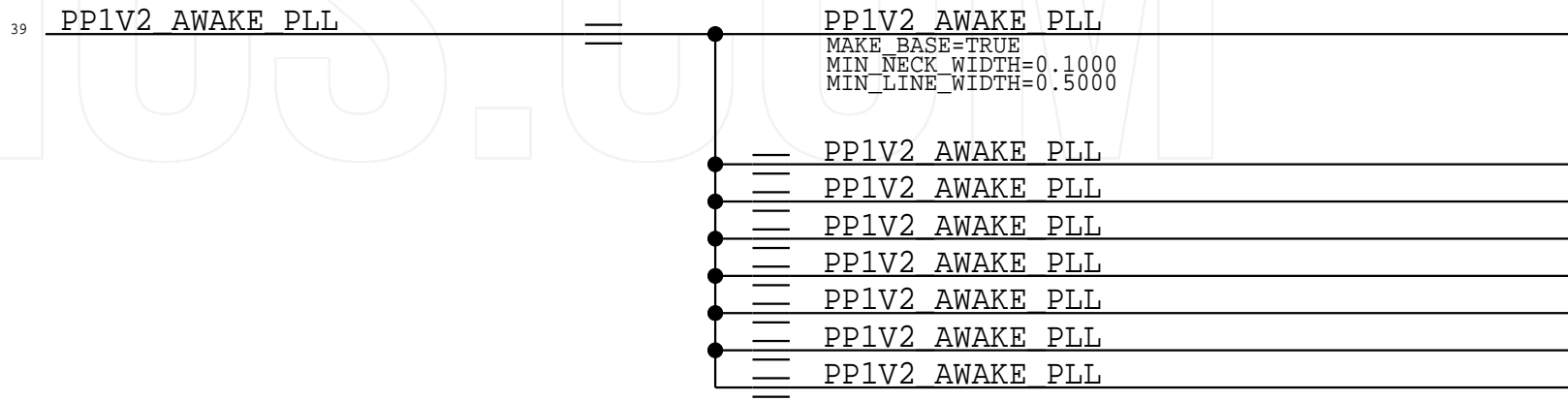
SPMU LDO 6



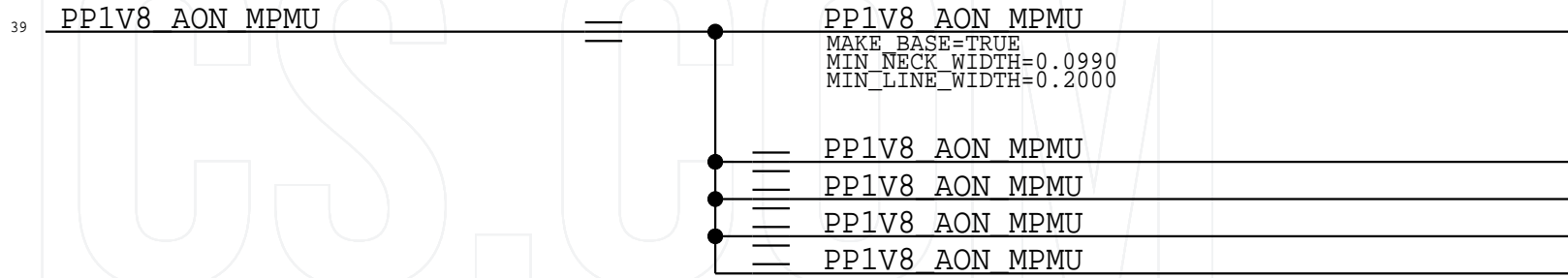
MPMU LDO 7



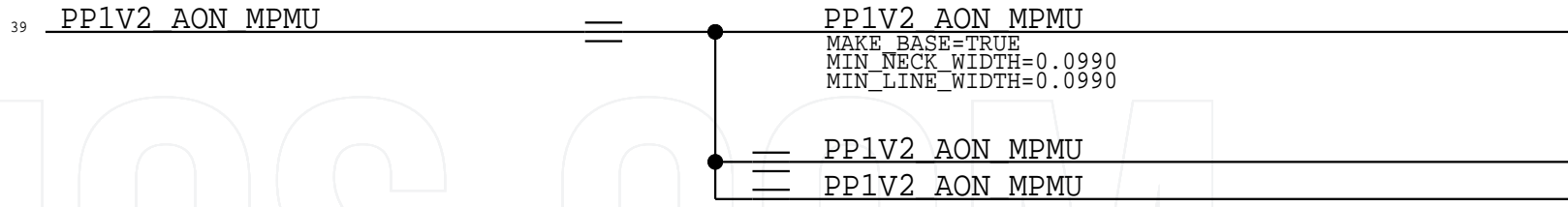
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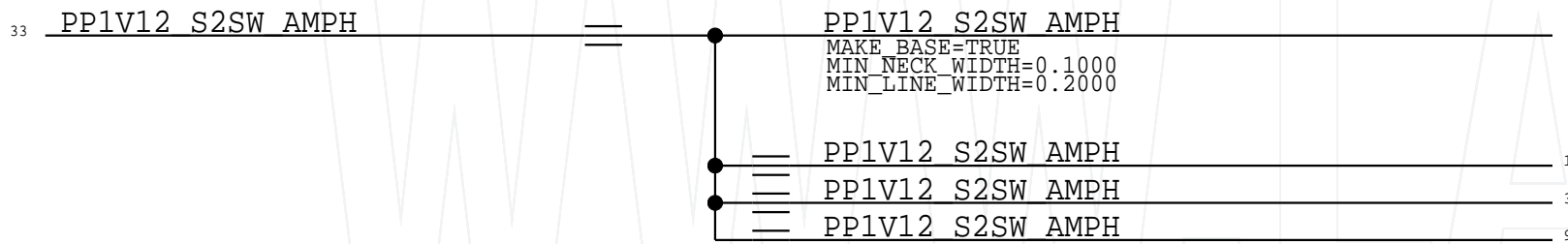
MPMU LDO 9



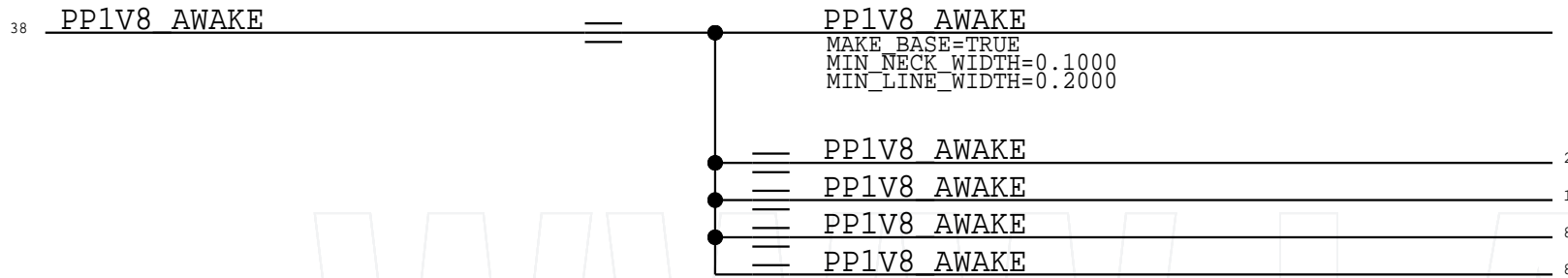
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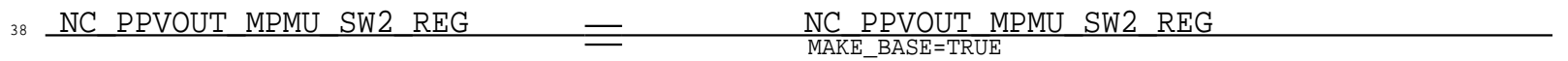
SPMU BUCK 14



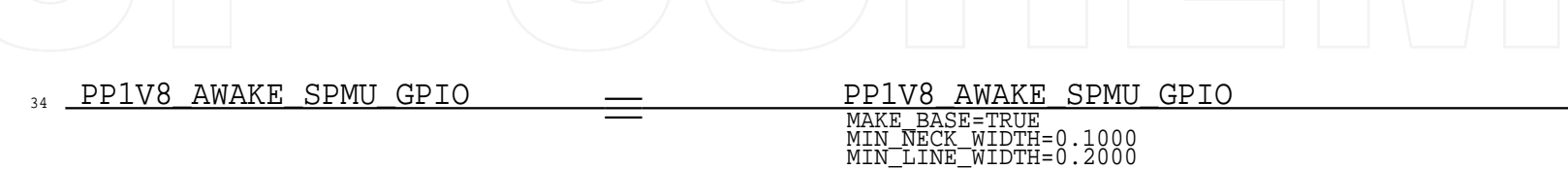
MPMU BUCK 3 SW 1



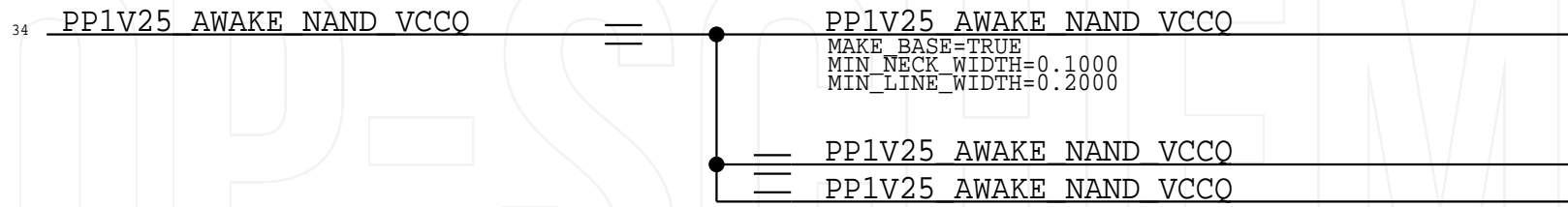
MPMU BUCK 3 SW 2



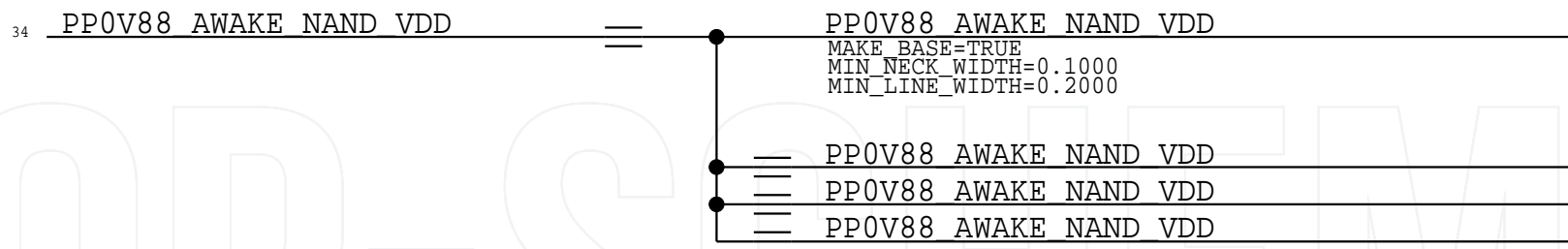
SPMU BUCK 3 SW 4



SPMU BUCK 13 SW 5



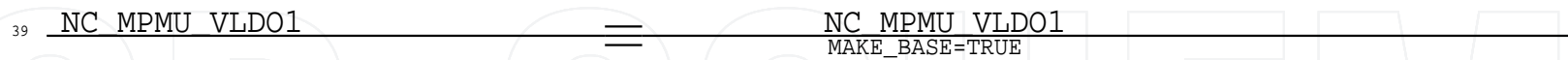
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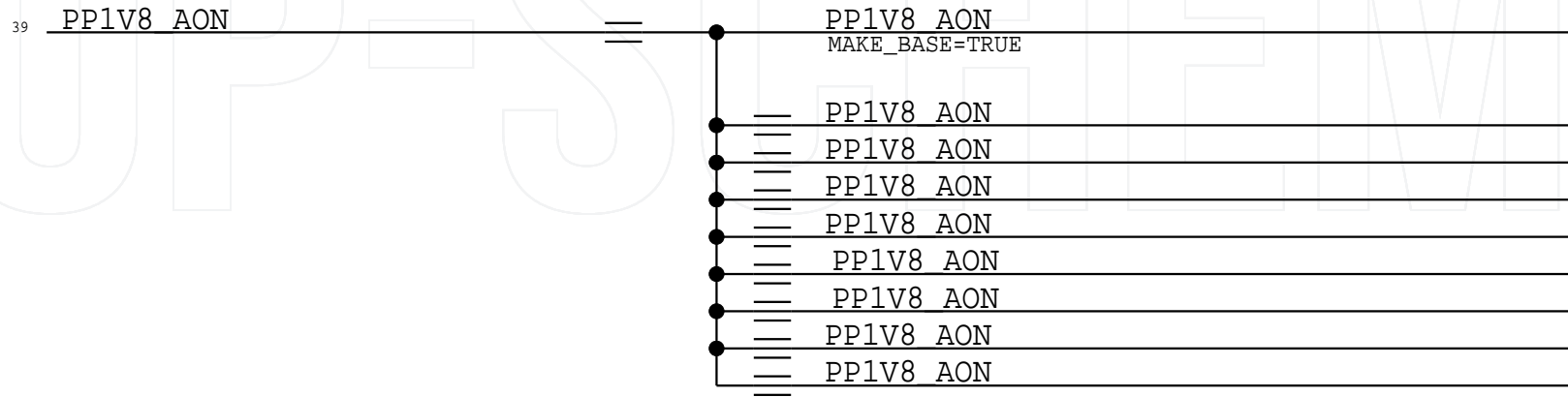
SPMU BUCK 12 SW 7

TIED TO SW6

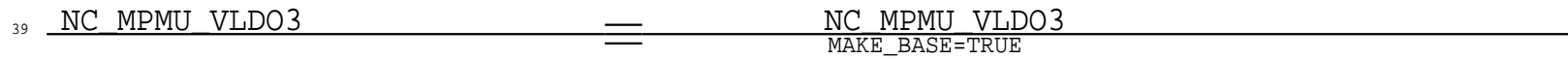
MPMU LDO 1




MPMU LDO 2



MPMU LDO 3



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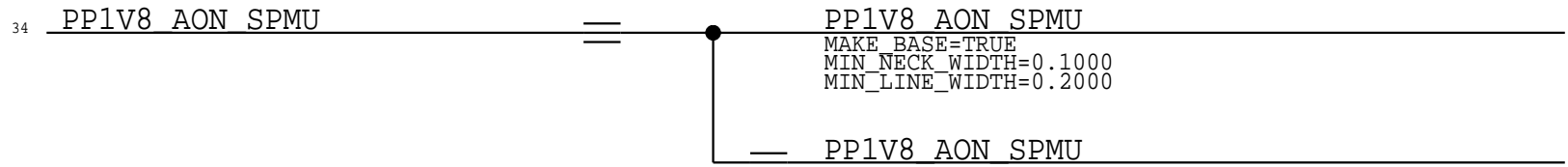
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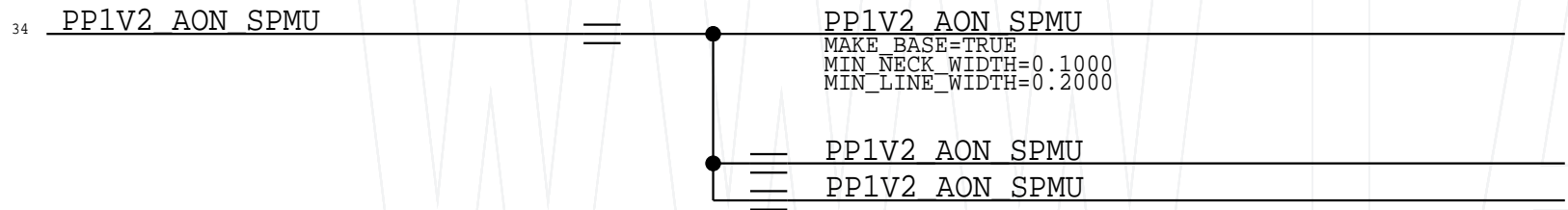
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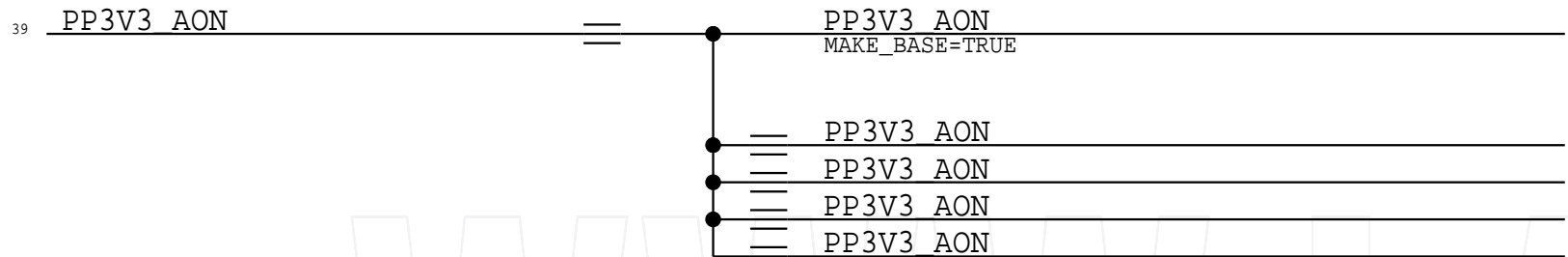
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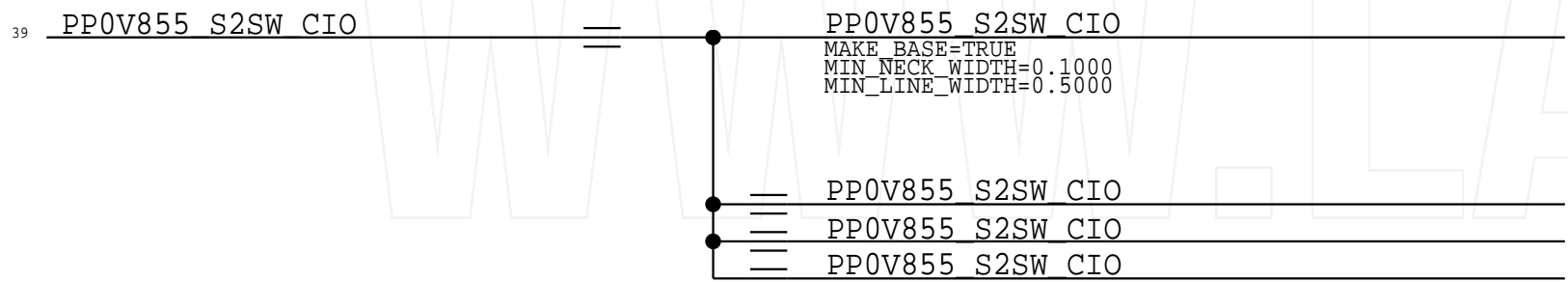
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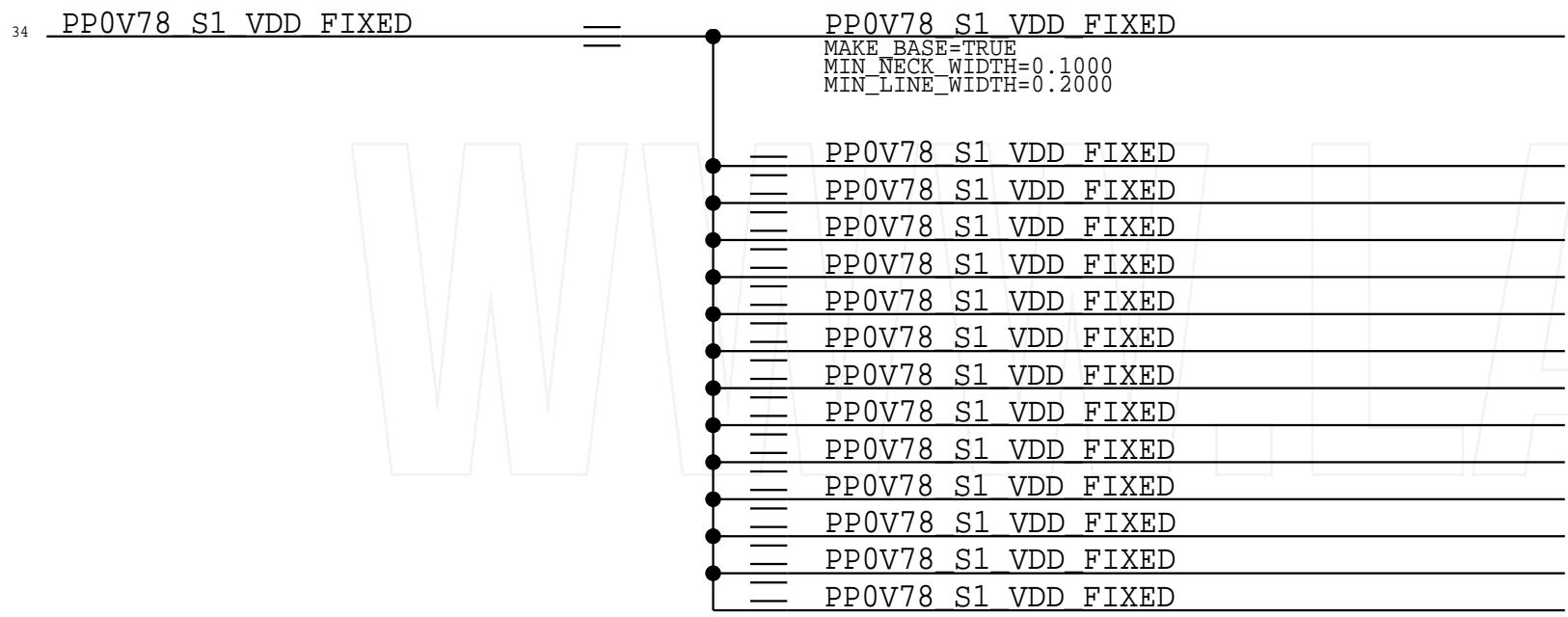
MPMU LDO 10



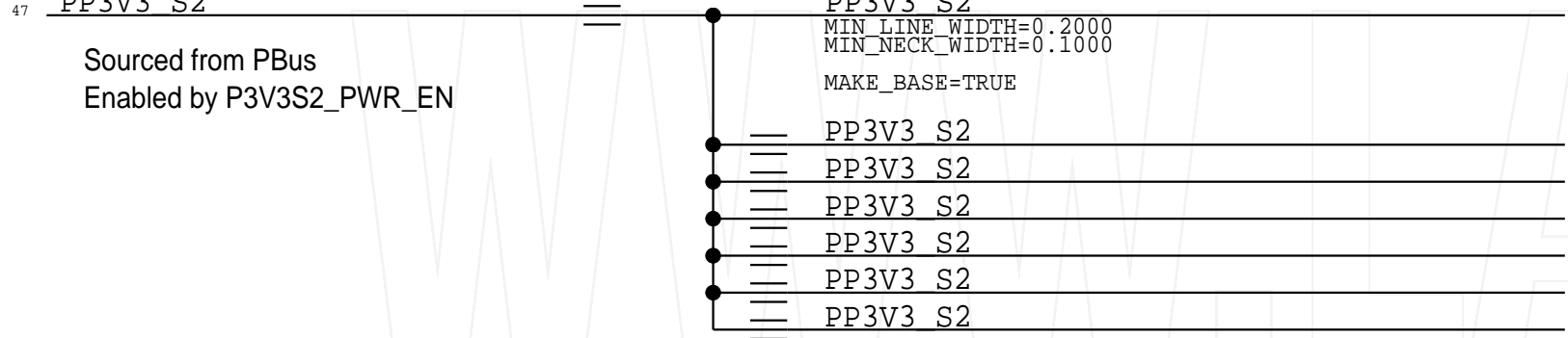
MPMU LDO 11



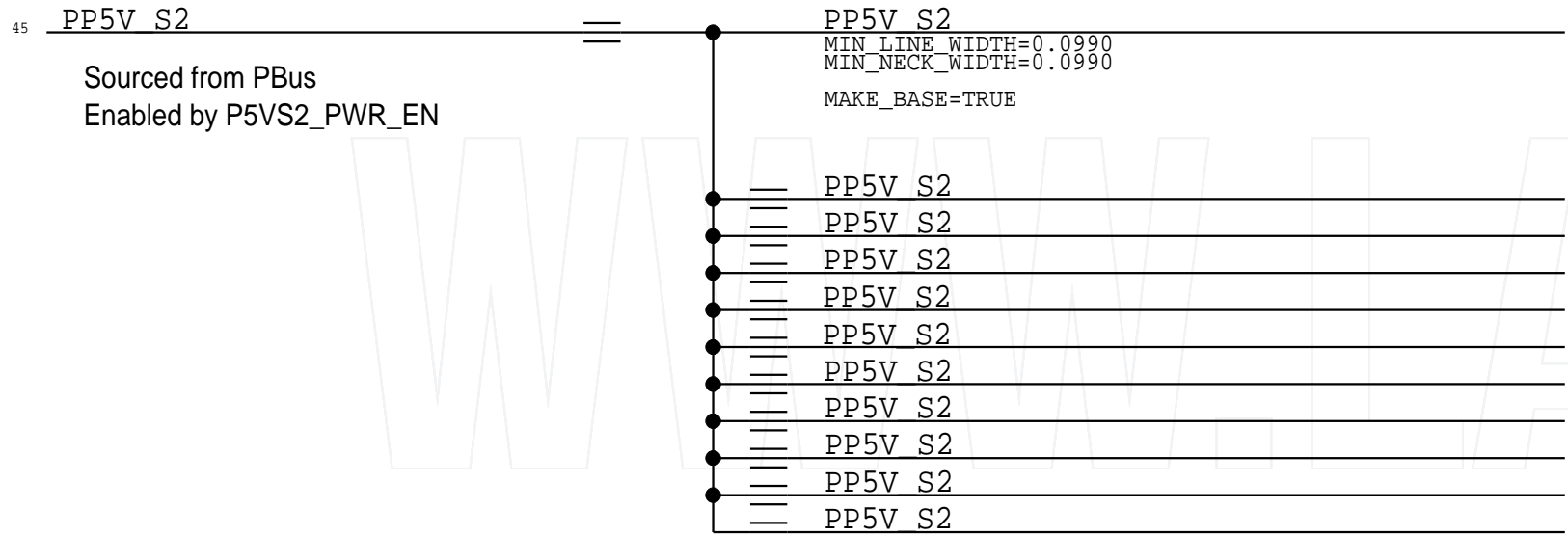
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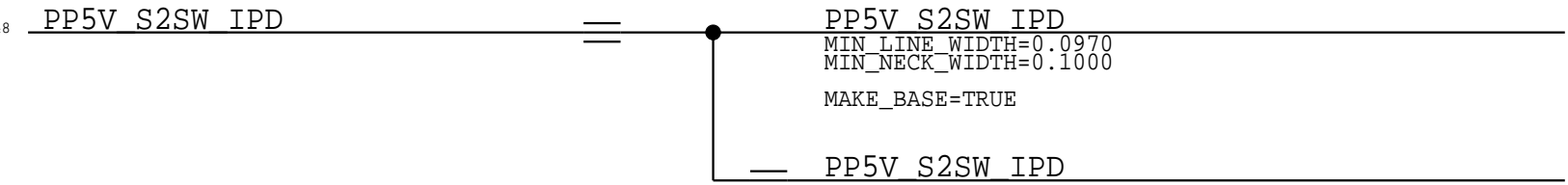
UC710 - 3V3_S2



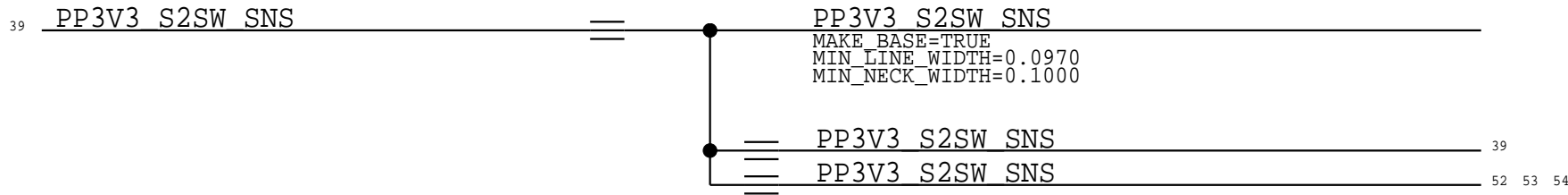
UC300 - 5V S2



Trackpad - 5V S2



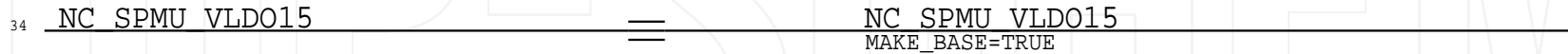
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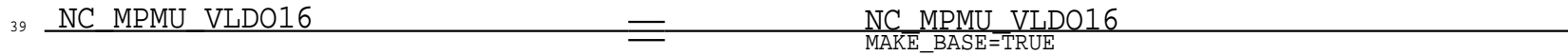
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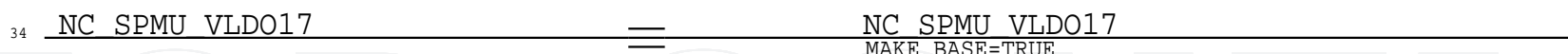
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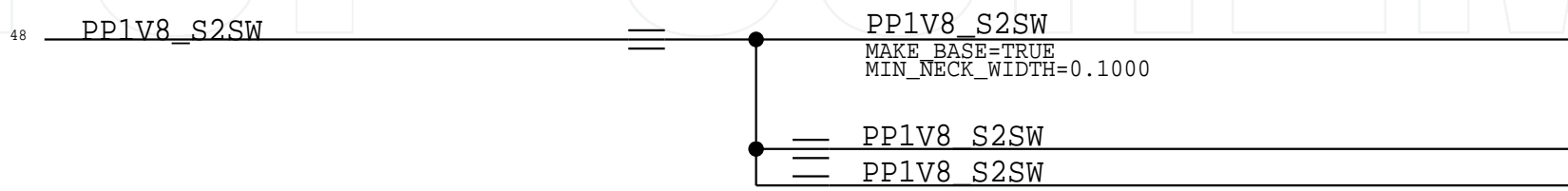
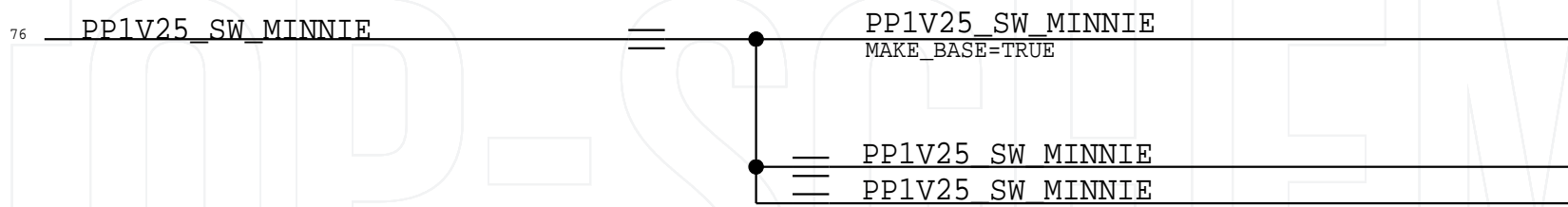
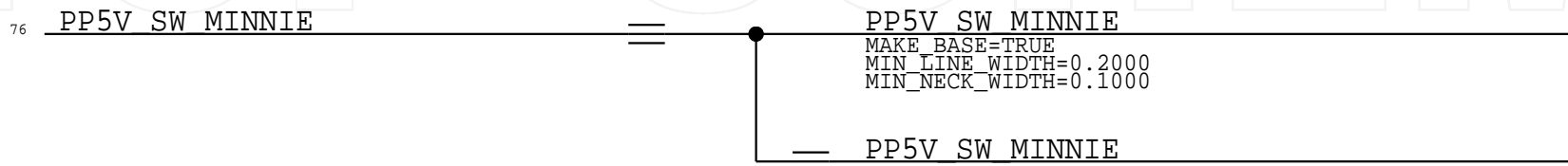
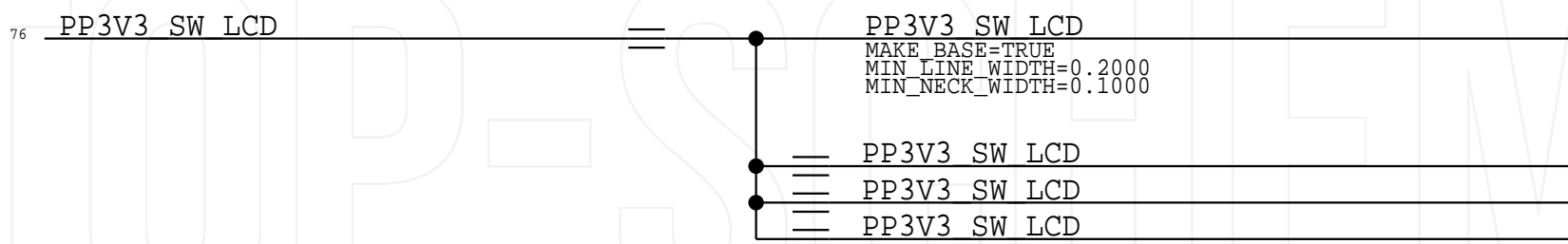
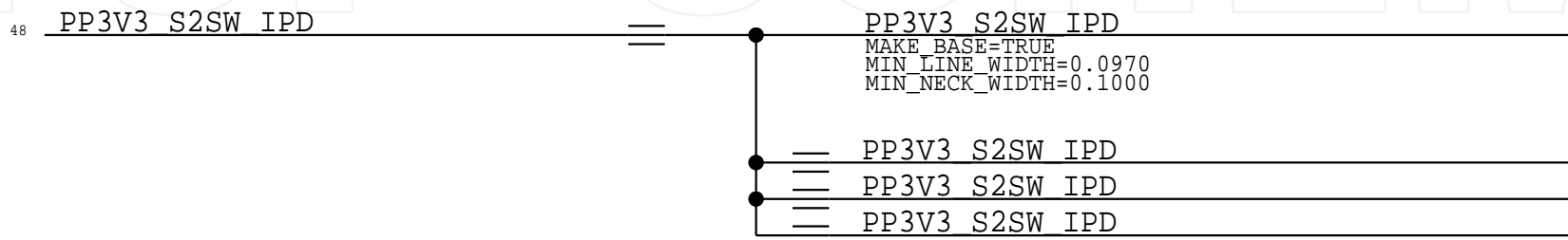
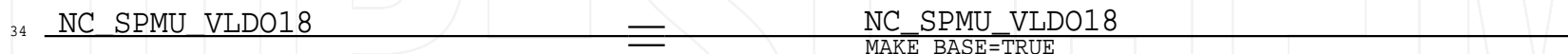
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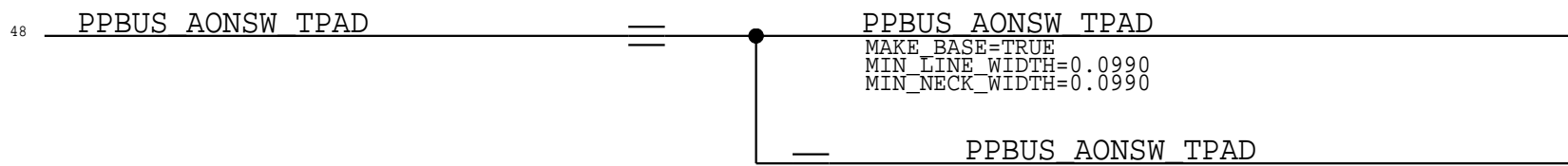
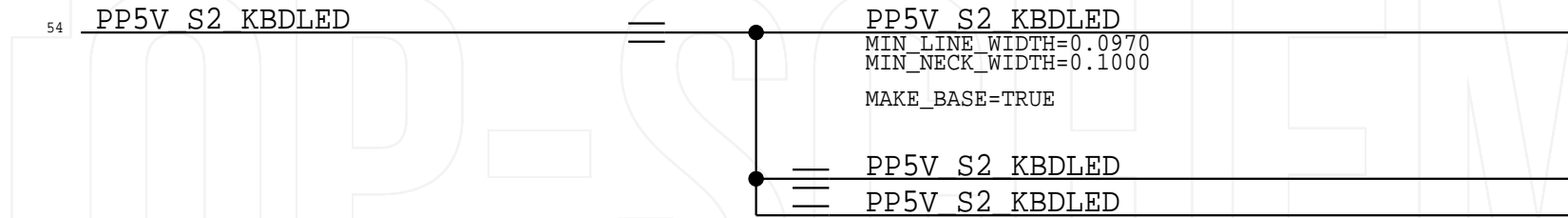
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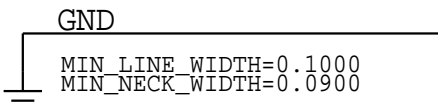
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Keyboard Backlight - 5V S2



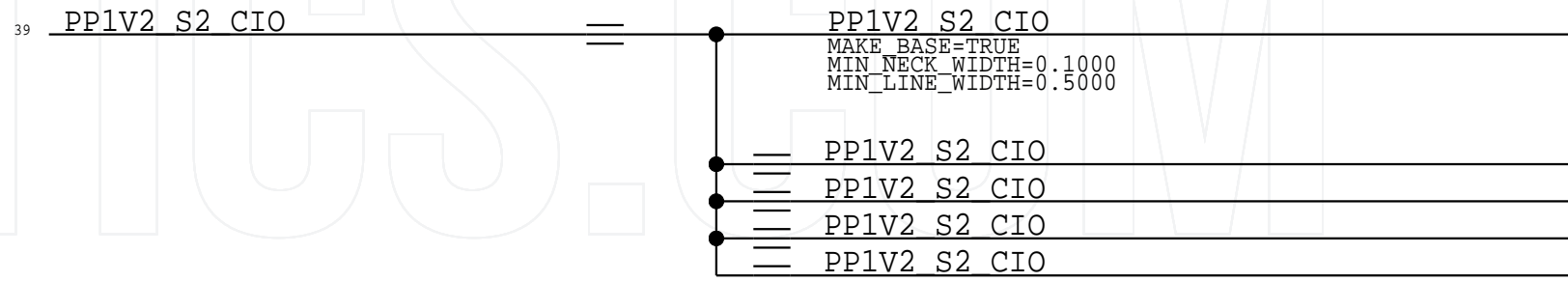
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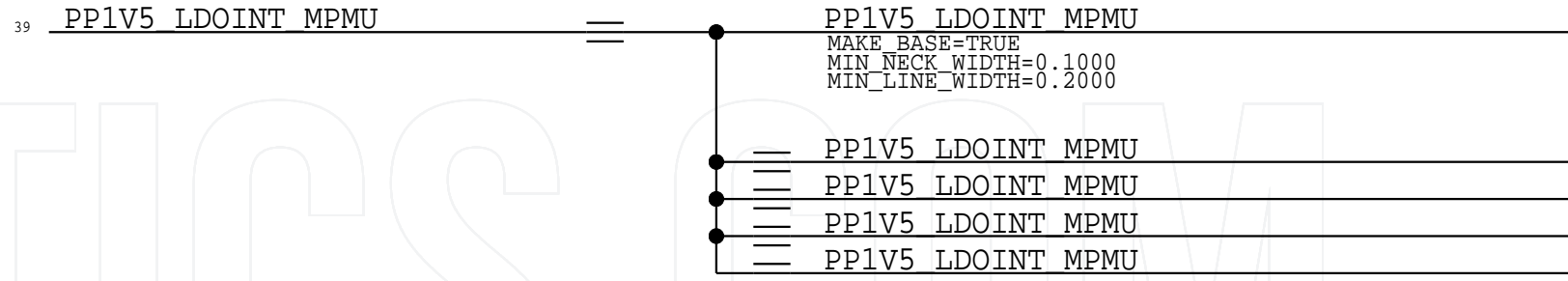
MPMU LDO19

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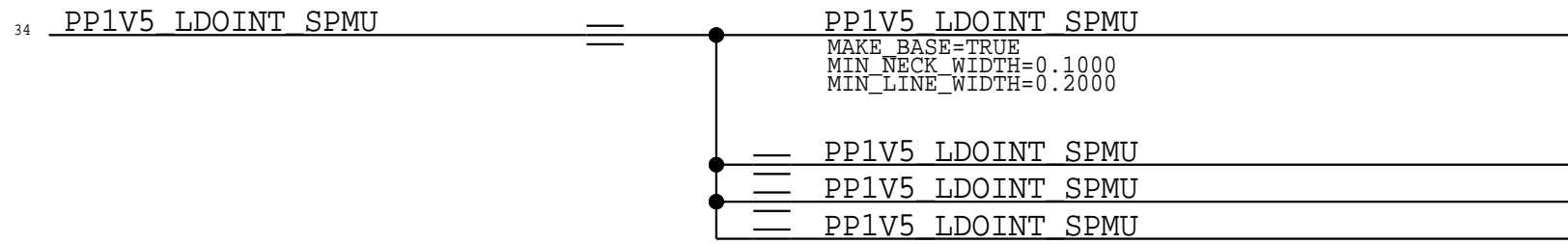
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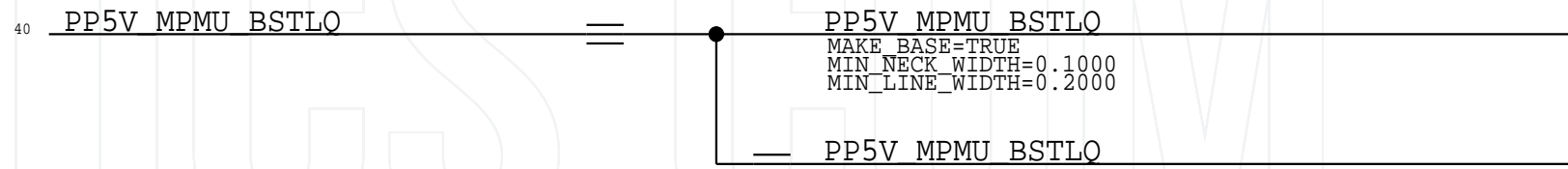
MPMU LDOINT



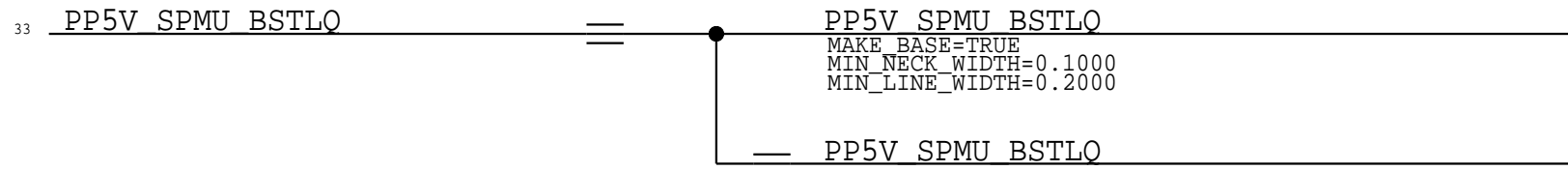
SPMU LDOINT



MPMU VDD BOOST



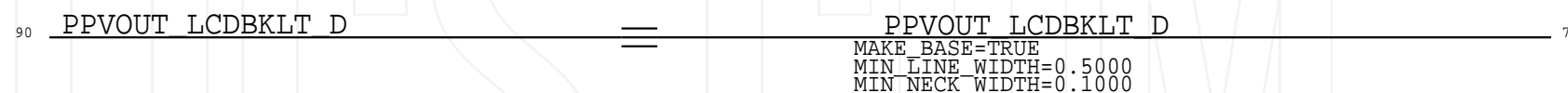
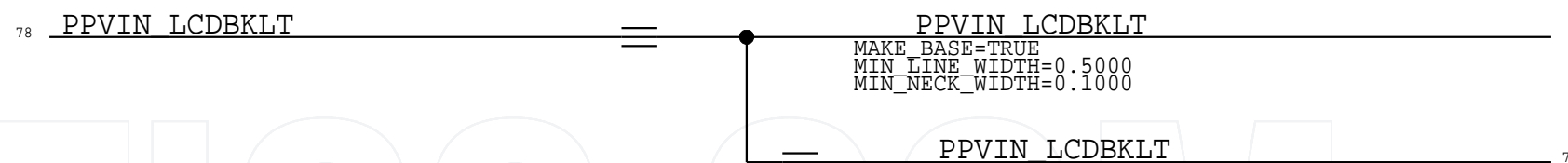
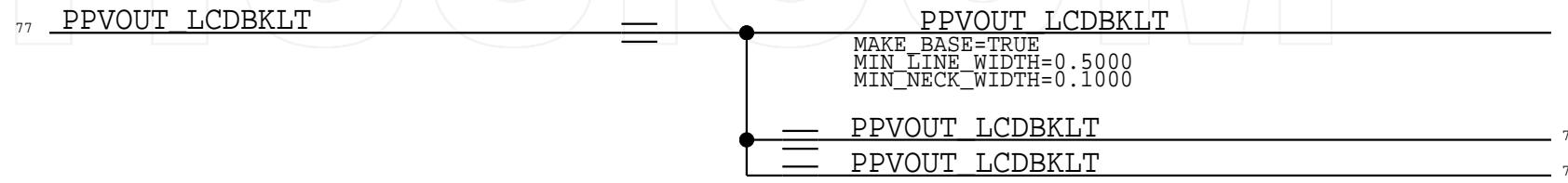
SPMU VDD BOOST



MPMU LDO RTC

SHORTED TO MPMU LDOINT FOR PORTABLES

Display Backlight Rails



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A Lid Angle Sensor Aliases

85	AMR_LEFT_OR_ND_1V8	MAKE_BASE=TRUE	AMR_LEFT_OR_ND_1V8	41
			AMR_LEFT_OR_ND_1V8	81

B Speaker Amplifier Aliases

9	TDM_SPKRAMP_L_D2R	MAKE_BASE=TRUE	TDM_SPKRAMP_L_D2R	82
			TDM_SPKRAMP_L_D2R	42
9	TDM_SPKRAMP_R_D2R	MAKE_BASE=TRUE	TDM_SPKRAMP_R_D2R	43
			TDM_SPKRAMP_R_D2R	83

C PMU Aliases

35	SWD_NUB_SWCLK_SPMU	MAKE_BASE=TRUE	SWD_NUB_SWCLK_SPMU	12
35	SWD_NUB_SWDIO_SPMU	MAKE_BASE=TRUE	SWD_NUB_SWDIO_SPMU	12
41	SWD_NUB_SWCLK_MPMU	MAKE_BASE=TRUE	SWD_NUB_SWCLK_MPMU	12
41	SWD_NUB_SWDIO_MPMU	MAKE_BASE=TRUE	SWD_NUB_SWDIO_MPMU	12
76	PMU_SYS_ALIVE	MAKE_BASE=TRUE	PMU_SYS_ALIVE	41 42 75

D Charger Aliases

26	P5VS2_PGOOD	MAKE_BASE=TRUE	P5VS2_PGOOD	45
25	NC_CHGR_CBC_ON	MAKE_BASE=TRUE	NC_CHGR_CBC_ON	
25	NC_CHGR_EN_VR1	MAKE_BASE=TRUE	NC_CHGR_EN_VR1	
25	NC_CHGR_SMC_RST_L	MAKE_BASE=TRUE	NC_CHGR_SMC_RST_L	

E PP5V_S2 Aliases

26	P5VS2_PWR_EN	MAKE_BASE=TRUE	P5VS2_PWR_EN	45 46 48
45	P5VS2_EN	MAKE_BASE=TRUE	P5VS2_EN	45

F Display Aliases

75	UART_TCON_D2R	MAKE_BASE=TRUE	UART_TCON_D2R	8
71	NC_BKLT_ISET_KEYB	MAKE_BASE=TRUE	NC_BKLT_ISET_KEYB	
71	NC_BKLT_KEYB1	MAKE_BASE=TRUE	NC_BKLT_KEYB1	
71	NC_BKLT_KEYB2	MAKE_BASE=TRUE	NC_BKLT_KEYB2	
71	NC_KBDBKLT_SW2	MAKE_BASE=TRUE	NC_KBDBKLT_SW2	
71	NC_VOUT_KEYBDLED_FB2	MAKE_BASE=TRUE	NC_VOUT_KEYBDLED_FB2	
71	UNUSED_LP8548_PWM	MAKE_BASE=TRUE	UNUSED_LP8548_PWM	

G Secure Element Aliases


23	NC_SE_GPIO0	MAKE_BASE=TRUE	NC_SE_GPIO0	
23	NC_I2C_SE_SCL	MAKE_BASE=TRUE	NC_I2C_SE_SCL	
23	NC_I2C_SE_SDA	MAKE_BASE=TRUE	NC_I2C_SE_SDA	

H NAND Aliases

71	NC_NAND0_S5E0_VPP	MAKE_BASE=TRUE	NC_NAND0_S5E0_VPP	
72	NC_NAND0_S5E1_VPP	MAKE_BASE=TRUE	NC_NAND0_S5E1_VPP	

I Wireless Module Aliases

70 69	NC_RF_BT_DED	MAKE_BASE=TRUE	NC_RF_BT_DED	
	TPT_WLAN_JTAG_TCK	MAKE_BASE=TRUE	TPT_WLAN_JTAG_TCK	69 70
	TPT_WLAN_JTAG_TMS	MAKE_BASE=TRUE	TPT_WLAN_JTAG_TMS	69 70
	TPT_WLAN_JTAG_TRSTN	MAKE_BASE=TRUE	TPT_WLAN_JTAG_TRSTN	69
	TPT_WLAN_JTAG_TDI	MAKE_BASE=TRUE	TPT_WLAN_JTAG_TDI	69

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G USB-C Aliases: GPIO

59	TP_ATCRTMR0_GPIO_0	==	MAKE_BASE+TRUE	TP_ATCRTMR0_GPIO_0	
59	NC_ATCRTMR0_GPIO_1	==	MAKE_BASE+TRUE	NC_ATCRTMR0_GPIO_1	
59	TP_ATCRTMR0_GPIO_2	==	MAKE_BASE+TRUE	TP_ATCRTMR0_GPIO_2	
59	TP_ATCRTMR0_GPIO_3	==	MAKE_BASE+TRUE	TP_ATCRTMR0_GPIO_3	
60	TP_ATCRTMR1_GPIO_0	==	MAKE_BASE+TRUE	TP_ATCRTMR1_GPIO_0	
60	NC_ATCRTMR1_GPIO_1	==	MAKE_BASE+TRUE	NC_ATCRTMR1_GPIO_1	
60	TP_ATCRTMR1_GPIO_2	==	MAKE_BASE+TRUE	TP_ATCRTMR1_GPIO_2	
60	TP_ATCRTMR1_GPIO_3	==	MAKE_BASE+TRUE	TP_ATCRTMR1_GPIO_3	

Leave these as TP, so that RT13 debug modes can be enabled.

H USB-C Aliases: VDD I/O Fuse I/F

68	ATCRTMR0_VDDIO_EFUSE	==	MAKE_BASE+TRUE	ATCRTMR0_VDDIO_EFUSE	
68	ATCRTMR1_VDDIO_EFUSE	==	MAKE_BASE+TRUE	ATCRTMR1_VDDIO_EFUSE	

I USB-C Aliases: SOC Dock Connect

62	SOC_DOCK_CONNECT	==	MAKE_BASE+TRUE	SOC_DOCK_CONNECT	7
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J USB-C Aliases: UPC I2C

28	I2C_UPC01_3V3_SDA	==	MAKE_BASE+TRUE	I2C_UPC01_3V3_SDA	61 68
28	I2C_UPC01_3V3_SCL	==	MAKE_BASE+TRUE	I2C_UPC01_3V3_SCL	61 68

A USB-C Aliases: USB 2.0 I/F

65	USB2_ATC0_LS_P	==	MAKE_BASE+TRUE	USB2_ATC0_LS_P	68
65	USB2_ATC0_LS_N	==	MAKE_BASE+TRUE	USB2_ATC0_LS_N	68
65	USB2_ATC1_LS_P	==	MAKE_BASE+TRUE	USB2_ATC1_LS_P	68
65	USB2_ATC1_LS_N	==	MAKE_BASE+TRUE	USB2_ATC1_LS_N	68
65	USB_DBG_LS_P	==	MAKE_BASE+TRUE	USB_DBG_LS_P	62
65	USB_DBG_LS_N	==	MAKE_BASE+TRUE	USB_DBG_LS_N	62

B USB-C Aliases: CIO Debug I/F

	CIO_ATC0_LSRX	==	MAKE_BASE+TRUE	CIO_ATC0_LSRX	6 59
	CIO_ATC0_LSTX	==	MAKE_BASE+TRUE	CIO_ATC0_LSTX	6 59
	CIO_ATC1_LSRX	==	MAKE_BASE+TRUE	CIO_ATC1_LSRX	6 60
	CIO_ATC1_LSTX	==	MAKE_BASE+TRUE	CIO_ATC1_LSTX	6 60

C USB-C Aliases: EUSB I/F

65	EUSB_ATC0_P	==	MAKE_BASE+TRUE	EUSB_ATC0_P	6 13
65	EUSB_ATC0_N	==	MAKE_BASE+TRUE	EUSB_ATC0_N	6 13
65	EUSB_ATC1_P	==	MAKE_BASE+TRUE	EUSB_ATC1_P	6 13
65	EUSB_ATC1_N	==	MAKE_BASE+TRUE	EUSB_ATC1_N	6 13
13 7	EUSB_DBG_P	==	MAKE_BASE+TRUE	EUSB_DBG_P	65
13 7	EUSB_DBG_N	==	MAKE_BASE+TRUE	EUSB_DBG_N	65
65	ATCRTMR0_RESET_1V2_L	==	MAKE_BASE+TRUE	ATCRTMR0_RESET_1V2_L	62 66

D USB-C Aliases: I2C I/F


59	I2C_UPC0_ATCRTMR0_SDA_1V2	==	MAKE_BASE+TRUE	I2C_UPC0_ATCRTMR0_SDA_1V2	61 68
65	I2C_UPC0_ATCRTMR0_SDA_1V2	==	MAKE_BASE+TRUE	I2C_UPC0_ATCRTMR0_SDA_1V2	61 68
59	I2C_UPC0_ATCRTMR0_SCL_1V2	==	MAKE_BASE+TRUE	I2C_UPC0_ATCRTMR0_SCL_1V2	61 68
65	I2C_UPC0_ATCRTMR0_SCL_1V2	==	MAKE_BASE+TRUE	I2C_UPC0_ATCRTMR0_SCL_1V2	61 68
60	I2C_UPC1_ATCRTMR1_SDA_1V2	==	MAKE_BASE+TRUE	I2C_UPC1_ATCRTMR1_SDA_1V2	61 68
65	I2C_UPC1_ATCRTMR1_SDA_1V2	==	MAKE_BASE+TRUE	I2C_UPC1_ATCRTMR1_SDA_1V2	61 68
60	I2C_UPC1_ATCRTMR1_SCL_1V2	==	MAKE_BASE+TRUE	I2C_UPC1_ATCRTMR1_SCL_1V2	61 68
65	I2C_UPC1_ATCRTMR1_SCL_1V2	==	MAKE_BASE+TRUE	I2C_UPC1_ATCRTMR1_SCL_1V2	61 68

E USB-C Aliases: SWD I/F

59	SWD_NUB_ATCRTMR_SWCLK	==	MAKE_BASE+TRUE	SWD_NUB_ATCRTMR_SWCLK	13
60	SWD_NUB_ATCRTMR_SWCLK	==	MAKE_BASE+TRUE	SWD_NUB_ATCRTMR_SWCLK	13
59	SWD_NUB_ATCRTMR_SWDIO	==	MAKE_BASE+TRUE	SWD_NUB_ATCRTMR_SWDIO	13
60	SWD_NUB_ATCRTMR_SWDIO	==	MAKE_BASE+TRUE	SWD_NUB_ATCRTMR_SWDIO	13

F USB-C Aliases: CC I/F

97	NC_USBC0_CC_FLT_L	==	MAKE_BASE+TRUE	NC_USBC0_CC_FLT_L	62 97
97	NC_USBC1_CC_FLT_L	==	MAKE_BASE+TRUE	NC_USBC1_CC_FLT_L	62 97

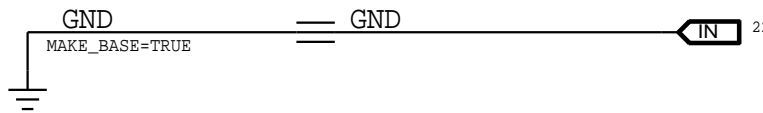
Signal Aliases 2		
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C DEBUG ALIAS

7	NC AON_SLEEP1_RESET_L	==	NC AON_SLEEP1_RESET_L
	MAKE_BASE=TRUE		MAKE_BASE=TRUE
7	NC_SOC_SWD_TMS3	==	NC_SOC_SWD_TMS3
	MAKE_BASE=TRUE		MAKE_BASE=TRUE
7	NC_SWD_R1_SWDIO	==	NC_SWD_R1_SWDIO
	MAKE_BASE=TRUE		MAKE_BASE=TRUE

D GND ALIAS

The DUT_GND_DETECT signal is for dev only,
and should be tied to GND.



A GPIO AOP ALIAS

8	NC_SOC_AOP_I2CM1_SCL	==	NC_SOC_AOP_I2CM1_SCL
	MAKE_BASE=TRUE		MAKE_BASE=TRUE
8	NC_SOC_AOP_I2CM1_SDA	==	NC_SOC_AOP_I2CM1_SDA
	MAKE_BASE=TRUE		MAKE_BASE=TRUE
8	NC_SOC_AOP_I2CM2_SCL	==	NC_SOC_AOP_I2CM2_SCL
	MAKE_BASE=TRUE		MAKE_BASE=TRUE
8	NC_SOC_AOP_I2CM2_SDA	==	NC_SOC_AOP_I2CM2_SDA
	MAKE_BASE=TRUE		MAKE_BASE=TRUE
98 8	NC_AOP_I2S0_LRCLK	==	NC_AOP_I2S0_LRCLK
	MAKE_BASE=TRUE		MAKE_BASE=TRUE
98 8	NC_AOP_I2S0_LRCLK	==	NC_AOP_I2S0_LRCLK
	MAKE_BASE=TRUE		MAKE_BASE=TRUE
8	NC_SOC_AOP_UART0_RXD	==	NC_SOC_AOP_UART0_RXD
	MAKE_BASE=TRUE		MAKE_BASE=TRUE
8	NC_SOC_AOP_UART0_TXD	==	NC_SOC_AOP_UART0_TXD
	MAKE_BASE=TRUE		MAKE_BASE=TRUE
8	NC_SOC_AOP_UART1_RXD	==	NC_SOC_AOP_UART1_RXD
	MAKE_BASE=TRUE		MAKE_BASE=TRUE
8	NC_SOC_AOP_UART1_TXD	==	NC_SOC_AOP_UART1_TXD
	MAKE_BASE=TRUE		MAKE_BASE=TRUE
8	NC_SOC_AOP_UART2_RXD	==	NC_SOC_AOP_UART2_RXD
	MAKE_BASE=TRUE		MAKE_BASE=TRUE
8	NC_SOC_AOP_UART2_TXD	==	NC_SOC_AOP_UART2_TXD
	MAKE_BASE=TRUE		MAKE_BASE=TRUE
8	NC_AOP_FUNC0	==	NC_AOP_FUNC0
	MAKE_BASE=TRUE		MAKE_BASE=TRUE
8	NC_AOP_FUNC1	==	NC_AOP_FUNC1
	MAKE_BASE=TRUE		MAKE_BASE=TRUE
8	NC_AOP_FUNC2	==	NC_AOP_FUNC2
	MAKE_BASE=TRUE		MAKE_BASE=TRUE
8	NC_AOP_FUNC3	==	NC_AOP_FUNC3
	MAKE_BASE=TRUE		MAKE_BASE=TRUE
8	NC_AOP_FUNC11	==	NC_AOP_FUNC11
	MAKE_BASE=TRUE		MAKE_BASE=TRUE
8	NC_AOP_FUNC12	==	NC_AOP_FUNC12
	MAKE_BASE=TRUE		MAKE_BASE=TRUE
8	NC_AOP_FUNC20	==	NC_AOP_FUNC20
	MAKE_BASE=TRUE		MAKE_BASE=TRUE
8	NC_HDMI_CEC_AOP_TX	==	NC_HDMI_CEC_AOP_TX
	MAKE_BASE=TRUE		MAKE_BASE=TRUE
8	NC_HDMI_CEC_AOP_RX	==	NC_HDMI_CEC_AOP_RX
	MAKE_BASE=TRUE		MAKE_BASE=TRUE
8	NC_HDMI_HDP_AOP	==	NC_HDMI_HDP_AOP
	MAKE_BASE=TRUE		MAKE_BASE=TRUE
7	TP_SOC_DOCK_ATTENTION	==	TP_SOC_DOCK_ATTENTION
	MAKE_BASE=TRUE		MAKE_BASE=TRUE
8	NC_AOP_FUNC19	==	NC_AOP_FUNC19
	MAKE_BASE=TRUE		MAKE_BASE=TRUE
9	NC_TOUCHID_BKLT_PWM	==	NC_TOUCHID_BKLT_PWM
	MAKE_BASE=TRUE		MAKE_BASE=TRUE

B GPIO AP ALIAS

8	NC_BKLT_PWR_ON	==	NC_BKLT_PWR_ON
	MAKE_BASE=TRUE		MAKE_BASE=TRUE
8	NC_SOC_AP_GPIO_1	==	NC_SOC_AP_GPIO_1
	MAKE_BASE=TRUE		MAKE_BASE=TRUE
8	NC_CCG_I2C_INT	==	NC_CCG_I2C_INT
	MAKE_BASE=TRUE		MAKE_BASE=TRUE
8	NC_DMIC_ID	==	NC_DMIC_ID
	MAKE_BASE=TRUE		MAKE_BASE=TRUE
8	NC_SOC_AP_GPIO_18	==	NC_SOC_AP_GPIO_18
	MAKE_BASE=TRUE		MAKE_BASE=TRUE
8	NC_SOC_AP_GPIO_19	==	NC_SOC_AP_GPIO_19
	MAKE_BASE=TRUE		MAKE_BASE=TRUE
8	NC_ENET_I2C_LOM_INT_L	==	NC_ENET_I2C_LOM_INT_L
	MAKE_BASE=TRUE		MAKE_BASE=TRUE
8	NC_SOC_AP_GPIO_23	==	NC_SOC_AP_GPIO_23
	MAKE_BASE=TRUE		MAKE_BASE=TRUE
8	NC_SOC_AP_GPIO_24	==	NC_SOC_AP_GPIO_24
	MAKE_BASE=TRUE		MAKE_BASE=TRUE
8	NC_ENET_SELECT_1G_H_10G_L	==	NC_ENET_SELECT_1G_H_10G_L
	MAKE_BASE=TRUE		MAKE_BASE=TRUE
8	NC_SOC_AP_GPIO_26	==	NC_SOC_AP_GPIO_26
	MAKE_BASE=TRUE		MAKE_BASE=TRUE
8	NC_SOC_AP_UART1_CTS_L	==	NC_SOC_AP_UART1_CTS_L
	MAKE_BASE=TRUE		MAKE_BASE=TRUE
8	NC_SOC_AP_UART1_RTS_L	==	NC_SOC_AP_UART1_RTS_L
	MAKE_BASE=TRUE		MAKE_BASE=TRUE
8	NC_SOC_AP_UART1_RXD	==	NC_SOC_AP_UART1_RXD
	MAKE_BASE=TRUE		MAKE_BASE=TRUE
8	NC_SOC_AP_UART1_TXD	==	NC_SOC_AP_UART1_TXD
	MAKE_BASE=TRUE		MAKE_BASE=TRUE
8	NC_SOC_AP_UART3_CTS_L	==	NC_SOC_AP_UART3_CTS_L
	MAKE_BASE=TRUE		MAKE_BASE=TRUE
8	NC_SOC_AP_UART3_RTS_L	==	NC_SOC_AP_UART3_RTS_L
	MAKE_BASE=TRUE		MAKE_BASE=TRUE
8	NC_SOC_AP_UART3_RXD	==	NC_SOC_AP_UART3_RXD
	MAKE_BASE=TRUE		MAKE_BASE=TRUE
8	NC_SOC_AP_UART3_TXD	==	NC_SOC_AP_UART3_TXD
	MAKE_BASE=TRUE		MAKE_BASE=TRUE
8	NC_SOC_AP_UART4_RXD	==	NC_SOC_AP_UART4_RXD
	MAKE_BASE=TRUE		MAKE_BASE=TRUE
8	NC_SOC_AP_UART4_TXD	==	NC_SOC_AP_UART4_TXD
	MAKE_BASE=TRUE		MAKE_BASE=TRUE
8	NC_UART_TCON_R2D	==	NC_UART_TCON_R2D
	MAKE_BASE=TRUE		MAKE_BASE=TRUE
8	NC_UART_HDMI_D2R	==	NC_UART_HDMI_D2R
	MAKE_BASE=TRUE		MAKE_BASE=TRUE
8	NC_UART_HDMI_R2D	==	NC_UART_HDMI_R2D
	MAKE_BASE=TRUE		MAKE_BASE=TRUE
8	NC_SOC_AP_UART2_RXD	==	NC_SOC_AP_UART2_RXD
	MAKE_BASE=TRUE		MAKE_BASE=TRUE
8	NC_SOC_AP_UART2_TXD	==	NC_SOC_AP_UART2_TXD
	MAKE_BASE=TRUE		MAKE_BASE=TRUE
8	NC_SOC_AP_UART2_CTS_L	==	NC_SOC_AP_UART2_CTS_L
	MAKE_BASE=TRUE		MAKE_BASE=TRUE
8	NC_SOC_AP_UART2_RTS_L	==	NC_SOC_AP_UART2_RTS_L
	MAKE_BASE=TRUE		MAKE_BASE=TRUE

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A SPI & I2S ALIAS

9	NC TDM SPKRAMP TOP BCLK R	==	NC TDM SPKRAMP TOP BCLK R MAKE_BASE=TRUE
9	NC TDM SPKRAMP TOP D2R	==	NC TDM SPKRAMP TOP D2R MAKE_BASE=TRUE
9	NC TDM SPKRAMP TOP R2D R	==	NC TDM SPKRAMP TOP R2D R MAKE_BASE=TRUE
9	NC TDM SPKRAMP TOP FSYNC R	==	NC TDM SPKRAMP TOP FSYNC R MAKE_BASE=TRUE
9	NC SOC AP SPMI0 SCLK	==	NC SOC AP SPMI0 SCLK MAKE_BASE=TRUE
9	NC SOC AP SPMI0 SDATA	==	NC SOC AP SPMI0 SDATA MAKE_BASE=TRUE
9	NC SOC AP SPI5 MISO	==	NC SOC AP SPI5 MISO MAKE_BASE=TRUE
9	NC SOC AP SPI5 MOSI	==	NC SOC AP SPI5 MOSI MAKE_BASE=TRUE
9	NC SOC AP SPI5 SCLK	==	NC SOC AP SPI5 SCLK MAKE_BASE=TRUE
9	NC SOC AP SPI5 CS L	==	NC SOC AP SPI5 CS L MAKE_BASE=TRUE
9	NC SOC SSPI0 MISO	==	NC SOC SSPI0 MISO MAKE_BASE=TRUE
9	NC SOC SSPI0 MOSI	==	NC SOC SSPI0 MOSI MAKE_BASE=TRUE
9	NC SOC SSPI0 SCLK	==	NC SOC SSPI0 SCLK MAKE_BASE=TRUE
9	NC SOC SGPIO 1	==	NC SOC SGPIO 1 MAKE_BASE=TRUE
9	NC SOC AP SPI2 CS L	==	NC SOC AP SPI2 CS L MAKE_BASE=TRUE
99	NC SOC AP I2S0 MCK	==	NC SOC AP I2S0 MCK MAKE_BASE=TRUE
99	NC SOC AP I2S1 MCK	==	NC SOC AP I2S1 MCK MAKE_BASE=TRUE
99	NC SOC AP I2S2 MCK	==	NC SOC AP I2S2 MCK MAKE_BASE=TRUE
8	NC PDM DMIC DATA4	==	NC PDM DMIC DATA4 MAKE_BASE=TRUE
8	NC PDM DMIC CLK2 R	==	NC PDM DMIC CLK2 R MAKE_BASE=TRUE
8	NC AOP I2S0 BCLK	==	NC AOP I2S0 BCLK MAKE_BASE=TRUE
8	NC AOP I2S0 DIN	==	NC AOP I2S0 DIN MAKE_BASE=TRUE
8	NC AOP I2S0 DOUT	==	NC AOP I2S0 DOUT MAKE_BASE=TRUE
8	NC SOC AOP SPI1 CS L	==	NC SOC AOP SPI1 CS L MAKE_BASE=TRUE
99	NC SPI DP2HDMI HOLD L	==	NC SPI DP2HDMI HOLD L MAKE_BASE=TRUE
99	NC SOC AP I2S0 MCK	==	NC SOC AP I2S0 MCK MAKE_BASE=TRUE
99	NC SOC AP I2S1 MCK	==	NC SOC AP I2S1 MCK MAKE_BASE=TRUE
99	NC SOC AP I2S2 MCK	==	NC SOC AP I2S2 MCK MAKE_BASE=TRUE
99	NC SPI DP2HDMI HOLD L	==	NC SPI DP2HDMI HOLD L MAKE_BASE=TRUE
9	NC SOC SPI3 MOSI	==	NC SOC SPI3 MOSI MAKE_BASE=TRUE
9	NC SOC SPI3 MISO	==	NC SOC SPI3 MISO MAKE_BASE=TRUE
9	NC SOC SPI3 SCLK	==	NC SOC SPI3 SCLK MAKE_BASE=TRUE
9	NC SOC SPI3 SSIN	==	NC SOC SPI3 SSIN MAKE_BASE=TRUE
8	NC SOC GPIO16	==	NC SOC GPIO16 MAKE_BASE=TRUE
8	NC SOC GPIO17	==	NC SOC GPIO17 MAKE_BASE=TRUE

B GPIO MTP ALIAS

9	NC SOC MTP I2C0 SCL	==	NC SOC MTP I2C0 SCL MAKE_BASE=TRUE
9	NC SOC MTP I2C0 SDA	==	NC SOC MTP I2C0 SDA MAKE_BASE=TRUE
9	NC SOC MTP FUNC 6	==	NC SOC MTP FUNC 6 MAKE_BASE=TRUE
9	NC SOC MTP FUNC 7	==	NC SOC MTP FUNC 7 MAKE_BASE=TRUE
9	IPD MTP FUNC 1	==	IPD MTP FUNC 1 MAKE_BASE=TRUE
9	NC SOC MTP FUNC 2	==	NC SOC MTP FUNC 2 MAKE_BASE=TRUE


C AUDIO I2C

9	I2C SPKRAMP L SDA	==	I2C SPKRAMP L SDA MAKE_BASE=TRUE
9	I2C SPKRAMP L SCL	==	I2C SPKRAMP L SCL MAKE_BASE=TRUE
9	I2C SPKRAMP R CODEC SDA	==	I2C SPKRAMP R CODEC SDA MAKE_BASE=TRUE
9	I2C SPKRAMP R CODEC SCL	==	I2C SPKRAMP R CODEC SCL MAKE_BASE=TRUE

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A LPDP ALIAS

10	NC SOC LPDP RX AUX D1	==	NC SOC LPDP RX AUX D1 MAKE_BASE=TRUE
10	NC SOC LPDP RX AUX D2	==	NC SOC LPDP RX AUX D2 MAKE_BASE=TRUE
10	NC SOC LPDP RX AUX D3	==	NC SOC LPDP RX AUX D3 MAKE_BASE=TRUE
10	NC SOC LPDP RX AUX D4	==	NC SOC LPDP RX AUX D4 MAKE_BASE=TRUE
10	NC SOC LPDP RX AUX D5	==	NC SOC LPDP RX AUX D5 MAKE_BASE=TRUE
10	NC SOC LPDP RX AUX D6	==	NC SOC LPDP RX AUX D6 MAKE_BASE=TRUE
10	NC SOC LPDP RX AUX D7	==	NC SOC LPDP RX AUX D7 MAKE_BASE=TRUE
10	NC SOC LPDP RX AUX D8	==	NC SOC LPDP RX AUX D8 MAKE_BASE=TRUE
10	NC SOC LPDP RX AUX D9	==	NC SOC LPDP RX AUX D9 MAKE_BASE=TRUE
10	NC SOC LPDP RX AUX D10	==	NC SOC LPDP RX AUX D10 MAKE_BASE=TRUE
10	NC SOC LPDP RX AUX D11	==	NC SOC LPDP RX AUX D11 MAKE_BASE=TRUE
10	NC SOC ST PCIE PERST 1 L	==	NC SOC ST PCIE PERST 1 L MAKE_BASE=TRUE
10	NC SOC LPDP RX D1P	==	NC SOC LPDP RX D1P MAKE_BASE=TRUE
10	NC SOC LPDP RX D1N	==	NC SOC LPDP RX D1N MAKE_BASE=TRUE
10	NC SOC LPDP RX D2P	==	NC SOC LPDP RX D2P MAKE_BASE=TRUE
10	NC SOC LPDP RX D2N	==	NC SOC LPDP RX D2N MAKE_BASE=TRUE
10	NC SOC LPDP RX D3P	==	NC SOC LPDP RX D3P MAKE_BASE=TRUE
10	NC SOC LPDP RX D3N	==	NC SOC LPDP RX D3N MAKE_BASE=TRUE
10	NC SOC LPDP RX D4P	==	NC SOC LPDP RX D4P MAKE_BASE=TRUE
10	NC SOC LPDP RX D4N	==	NC SOC LPDP RX D4N MAKE_BASE=TRUE
10	NC SOC LPDP RX D5P	==	NC SOC LPDP RX D5P MAKE_BASE=TRUE
10	NC SOC LPDP RX D5N	==	NC SOC LPDP RX D5N MAKE_BASE=TRUE
10	NC SOC LPDP RX D6P	==	NC SOC LPDP RX D6P MAKE_BASE=TRUE
10	NC SOC LPDP RX D6N	==	NC SOC LPDP RX D6N MAKE_BASE=TRUE
10	NC SOC LPDP RX D7P	==	NC SOC LPDP RX D7P MAKE_BASE=TRUE
10	NC SOC LPDP RX D7N	==	NC SOC LPDP RX D7N MAKE_BASE=TRUE
10	NC SOC LPDP RX D8P	==	NC SOC LPDP RX D8P MAKE_BASE=TRUE
10	NC SOC LPDP RX D8N	==	NC SOC LPDP RX D8N MAKE_BASE=TRUE
10	NC SOC LPDP RX D9P	==	NC SOC LPDP RX D9P MAKE_BASE=TRUE
10	NC SOC LPDP RX D9N	==	NC SOC LPDP RX D9N MAKE_BASE=TRUE
10	NC SOC LPDP RX D10P	==	NC SOC LPDP RX D10P MAKE_BASE=TRUE
10	NC SOC LPDP RX D10N	==	NC SOC LPDP RX D10N MAKE_BASE=TRUE
10	NC SOC LPDP RX D11P	==	NC SOC LPDP RX D11P MAKE_BASE=TRUE
10	NC SOC LPDP RX D11N	==	NC SOC LPDP RX D11N MAKE_BASE=TRUE
10	NC LPDP EXT DATA CP<0>	==	NC LPDP EXT DATA CP<0> MAKE_BASE=TRUE
10	NC LPDP EXT DATA CN<0>	==	NC LPDP EXT DATA CN<0> MAKE_BASE=TRUE
10	NC LPDP EXT DATA CP<1>	==	NC LPDP EXT DATA CP<1> MAKE_BASE=TRUE
10	NC LPDP EXT DATA CN<1>	==	NC LPDP EXT DATA CN<1> MAKE_BASE=TRUE
10	NC LPDP EXT DATA CP<2>	==	NC LPDP EXT DATA CP<2> MAKE_BASE=TRUE
10	NC LPDP EXT DATA CN<2>	==	NC LPDP EXT DATA CN<2> MAKE_BASE=TRUE
10	NC LPDP EXT DATA CP<3>	==	NC LPDP EXT DATA CP<3> MAKE_BASE=TRUE
10	NC LPDP EXT DATA CN<3>	==	NC LPDP EXT DATA CN<3> MAKE_BASE=TRUE
10	NC LPDP EXT AUX CP	==	NC LPDP EXT AUX CP MAKE_BASE=TRUE
10	NC LPDP EXT AUX CN	==	NC LPDP EXT AUX CN MAKE_BASE=TRUE
10	NC LPDP EXT HPD	==	NC LPDP EXT HPD MAKE_BASE=TRUE
10	NC SOC LPDP RX1 RCAL POS	==	NC SOC LPDP RX1 RCAL POS MAKE_BASE=TRUE
10	NC SOC LPDP RX1 RCAL NEG	==	NC SOC LPDP RX1 RCAL NEG MAKE_BASE=TRUE

SYNC_MASTER=		SYNC_DATE=09/10/2021	
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A PCIe ALIAS

10	NC SOC GP PCIE RX1P	==	NC SOC GP PCIE RX1P MAKE_BASE=TRUE
10	NC SOC GP PCIE RX1N	==	NC SOC GP PCIE RX1N MAKE_BASE=TRUE
10	NC SOC GP PCIE TX1P	==	NC SOC GP PCIE TX1P MAKE_BASE=TRUE
10	NC SOC GP PCIE TX1N	==	NC SOC GP PCIE TX1N MAKE_BASE=TRUE
10	NC SOC GP PCIE CLK1 100MP	==	NC SOC GP PCIE CLK1 100MP MAKE_BASE=TRUE
10	NC SOC GP PCIE CLK1 100MN	==	NC SOC GP PCIE CLK1 100MN MAKE_BASE=TRUE
10	NC SOC GP PCIE CLKREQ 1 L	==	NC SOC GP PCIE CLKREQ 1 L MAKE_BASE=TRUE
10	NC SOC GP PCIE PERST 1 L	==	NC SOC GP PCIE PERST 1 L MAKE_BASE=TRUE
10	NC SOC GP PCIE RX2P	==	NC SOC GP PCIE RX2P MAKE_BASE=TRUE
10	NC SOC GP PCIE RX2N	==	NC SOC GP PCIE RX2N MAKE_BASE=TRUE
10	NC SOC GP PCIE TX2P	==	NC SOC GP PCIE TX2P MAKE_BASE=TRUE
10	NC SOC GP PCIE TX2N	==	NC SOC GP PCIE TX2N MAKE_BASE=TRUE
10	NC SOC GP PCIE CLK2 100MP	==	NC SOC GP PCIE CLK2 100MP MAKE_BASE=TRUE
10	NC SOC GP PCIE CLK2 100MN	==	NC SOC GP PCIE CLK2 100MN MAKE_BASE=TRUE
10	NC SOC GP PCIE CLKREQ 2 L	==	NC SOC GP PCIE CLKREQ 2 L MAKE_BASE=TRUE
10	NC SOC GP PCIE PERST 2 L	==	NC SOC GP PCIE PERST 2 L MAKE_BASE=TRUE
10	NC SOC GP PCIE RX3P	==	NC SOC GP PCIE RX3P MAKE_BASE=TRUE
10	NC SOC GP PCIE RX3N	==	NC SOC GP PCIE RX3N MAKE_BASE=TRUE
10	NC SOC GP PCIE TX3P	==	NC SOC GP PCIE TX3P MAKE_BASE=TRUE
10	NC SOC GP PCIE TX3N	==	NC SOC GP PCIE TX3N MAKE_BASE=TRUE
10	NC SOC GP PCIE CLK3 100MP	==	NC SOC GP PCIE CLK3 100MP MAKE_BASE=TRUE
10	NC SOC GP PCIE CLK3 100MN	==	NC SOC GP PCIE CLK3 100MN MAKE_BASE=TRUE
10	NC SOC GP PCIE CLKREQ 3 L	==	NC SOC GP PCIE CLKREQ 3 L MAKE_BASE=TRUE
10	NC SOC GP PCIE PERST 3 L	==	NC SOC GP PCIE PERST 3 L MAKE_BASE=TRUE

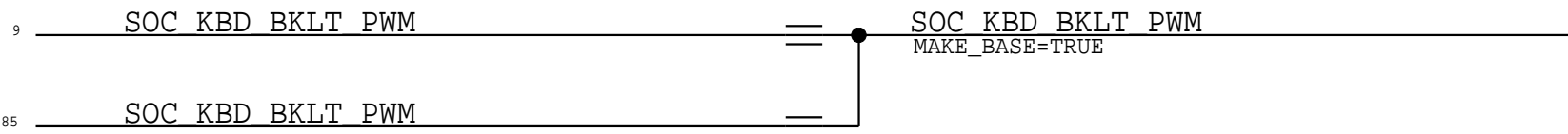
B DISP ALIAS

9	NC I2C SD DISP BKLT SCL	==	NC I2C SD DISP BKLT SCL MAKE_BASE=TRUE
9	NC I2C SD DISP BKLT SDA	==	NC I2C SD DISP BKLT SDA MAKE_BASE=TRUE
10	I2C DISP BKLT SCL	==	I2C DISP BKLT SCL MAKE_BASE=TRUE
10	I2C DISP BKLT SDA	==	I2C DISP BKLT SDA MAKE_BASE=TRUE
10	NC SPI DISP BKLT CLK R	==	NC SPI DISP BKLT CLK R MAKE_BASE=TRUE
10	NC SPI DISP BKLT CS L	==	NC SPI DISP BKLT CS L MAKE_BASE=TRUE
10	NC SPMI DISP BKLT CLK	==	NC SPMI DISP BKLT CLK MAKE_BASE=TRUE
10	NC SPMI DISP BKLT DATA	==	NC SPMI DISP BKLT DATA MAKE_BASE=TRUE
10	NC SOC DISP POL	==	NC SOC DISP POL MAKE_BASE=TRUE
10	NC DISP BKLT FSYNC	==	NC DISP BKLT FSYNC MAKE_BASE=TRUE
75	DISP BKLT LSYNC	==	DISP BKLT LSYNC MAKE_BASE=TRUE
10	NC SOC DISP TOUCH BSYNC 0	==	NC SOC DISP TOUCH BSYNC 0 MAKE_BASE=TRUE
10	NC SOC DISP TOUCH BSYNC 1	==	NC SOC DISP TOUCH BSYNC 1 MAKE_BASE=TRUE
10	NC SOC DISP TOUCH EB	==	NC SOC DISP TOUCH EB MAKE_BASE=TRUE
10	NC BKLT BOOST THROTTLE L	==	NC BKLT BOOST THROTTLE L MAKE_BASE=TRUE
10	NC SOC DFR DISP TE	==	NC SOC DFR DISP TE MAKE_BASE=TRUE
77	NC LCDBKLT FET DRV	==	NC LCDBKLT FET DRV MAKE_BASE=TRUE

D LPDP Aliases

10	NC SOC LPDP DP2HDMI RCAL POS	==	NC SOC LPDP DP2HDMI RCAL POS MAKE_BASE=TRUE
10	NC SOC LPDP DP2HDMI RCAL NEG	==	NC SOC LPDP DP2HDMI RCAL NEG MAKE_BASE=TRUE

C Keyboard Backlight



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A SMC & NUB ALIAS

NC SOC SMC GPIO 1	==	NC SOC SMC GPIO 1 MAKE_BASE=TRUE
NC SMC FAN 0 PWM	==	NC SMC FAN 0 PWM MAKE_BASE=TRUE
NC SMC FAN 0 TACH	==	NC SMC FAN 0 TACH MAKE_BASE=TRUE
NC SMC FAN 1 PWM	==	NC SMC FAN 1 PWM MAKE_BASE=TRUE
NC SMC FAN 1 TACH	==	NC SMC FAN 1 TACH MAKE_BASE=TRUE
NC SOC NUB CLK OUT 0	==	NC SOC NUB CLK OUT 0 MAKE_BASE=TRUE
NC SOC NUB GPIO 12	==	NC SOC NUB GPIO 12 MAKE_BASE=TRUE
NC ENET LOW PWR	==	NC ENET LOW PWR MAKE_BASE=TRUE
NC LOM PMU RESET EN	==	NC LOM PMU RESET EN MAKE_BASE=TRUE

B SENSE ALIAS

VSNS VDD PCPU	==	VSNS VDD PCPU MAKE_BASE=TRUE	55
VSNS VSS PCPU	==	VSNS VSS PCPU MAKE_BASE=TRUE	55
VSNS ABSMIN PCPU	==	VSNS ABSMIN PCPU MAKE_BASE=TRUE	55
VSNS VDD ECPU	==	VSNS VDD ECPU MAKE_BASE=TRUE	55
VSNS VDD GPU	==	VSNS VDD GPU MAKE_BASE=TRUE	55
VSNS VDD SOC	==	VSNS VDD SOC MAKE_BASE=TRUE	55
VSNS VDD DISP	==	VSNS VDD DISP MAKE_BASE=TRUE	55
VSNS VDD2H 1	==	VSNS VDD2H 1 MAKE_BASE=TRUE	55
VSNS VSS 1	==	VSNS VSS 1 MAKE_BASE=TRUE	55
VSNS VDD2H 2	==	VSNS VDD2H 2 MAKE_BASE=TRUE	55
VSNS VSS 2	==	VSNS VSS 2 MAKE_BASE=TRUE	55
VSNS VDDO S1	==	VSNS VDDO S1 MAKE_BASE=TRUE	55

C ISP ALIAS

NC SOC ISP GPIO 1	==	NC SOC ISP GPIO 1 MAKE_BASE=TRUE
NC SOC ISP GPIO 2	==	NC SOC ISP GPIO 2 MAKE_BASE=TRUE
NC SOC ISP GPIO 3	==	NC SOC ISP GPIO 3 MAKE_BASE=TRUE
NC SOC ISP SPMI0 SCLK	==	NC SOC ISP SPMI0 SCLK MAKE_BASE=TRUE
NC SOC ISP SPMI0 SDATA	==	NC SOC ISP SPMI0 SDATA MAKE_BASE=TRUE
NC SOC ISP SPMI1 SCLK	==	NC SOC ISP SPMI1 SCLK MAKE_BASE=TRUE
NC SOC ISP SPMI1 SDATA	==	NC SOC ISP SPMI1 SDATA MAKE_BASE=TRUE
NC SOC ISP I2C1 SCL	==	NC SOC ISP I2C1 SCL MAKE_BASE=TRUE
NC SOC ISP I2C1 SDA	==	NC SOC ISP I2C1 SDA MAKE_BASE=TRUE
NC SOC SENSOR0 CLK	==	NC SOC SENSOR0 CLK MAKE_BASE=TRUE
NC SOC SENSOR1 CLK	==	NC SOC SENSOR1 CLK MAKE_BASE=TRUE
NC SOC SENSOR2 CLK	==	NC SOC SENSOR2 CLK MAKE_BASE=TRUE
NC SOC SENSOR3 CLK	==	NC SOC SENSOR3 CLK MAKE_BASE=TRUE

D MIPI Aliases

NC SOC MIPI0C DPCLK	==	NC SOC MIPI0C DPCLK MAKE_BASE=TRUE
NC SOC MIPI0C DNCLK	==	NC SOC MIPI0C DNCLK MAKE_BASE=TRUE
NC SOC MIPI0C DPDATA<0>	==	NC SOC MIPI0C DPDATA<0> MAKE_BASE=TRUE
NC SOC MIPI0C DNDATA<0>	==	NC SOC MIPI0C DNDATA<0> MAKE_BASE=TRUE
NC SOC MIPI0C DPDATA<1>	==	NC SOC MIPI0C DPDATA<1> MAKE_BASE=TRUE
NC SOC MIPI0C DNDATA<1>	==	NC SOC MIPI0C DNDATA<1> MAKE_BASE=TRUE
NC SOC MIPI1C DPCLK	==	NC SOC MIPI1C DPCLK MAKE_BASE=TRUE
NC SOC MIPI1C DNCLK	==	NC SOC MIPI1C DNCLK MAKE_BASE=TRUE
NC SOC MIPI1C DPDATA<0>	==	NC SOC MIPI1C DPDATA<0> MAKE_BASE=TRUE
NC SOC MIPI1C DNDATA<0>	==	NC SOC MIPI1C DNDATA<0> MAKE_BASE=TRUE
NC SOC MIPI1C DPDATA<1>	==	NC SOC MIPI1C DPDATA<1> MAKE_BASE=TRUE
NC SOC MIPI1C DNDATA<1>	==	NC SOC MIPI1C DNDATA<1> MAKE_BASE=TRUE
NC SOC MIPID DPCLK	==	NC SOC MIPID DPCLK MAKE_BASE=TRUE
NC SOC MIPID DNCLK	==	NC SOC MIPID DNCLK MAKE_BASE=TRUE
NC SOC MIPID DPDATA<0>	==	NC SOC MIPID DPDATA<0> MAKE_BASE=TRUE
NC SOC MIPID DNDATA<0>	==	NC SOC MIPID DNDATA<0> MAKE_BASE=TRUE
NC SOC MIPI0C REXT	==	NC SOC MIPI0C REXT MAKE_BASE=TRUE
NC SOC MIPI1C REXT	==	NC SOC MIPI1C REXT MAKE_BASE=TRUE
NC SOC MIPID REXT	==	NC SOC MIPID REXT MAKE_BASE=TRUE

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SCSET RULES


DIELECTRIC BASED SPACING RULES	
RULE DEFINITION	LIST OF VALUES
A_DIELECTRIC_INX Calculates distance to nearest via hole	2-10
A_DIELECTRIC_INXD XX.VV.XX Calculates distance to nearest via hole (X and V are user defined)	2-10
A_DIELECTRIC_INXN_INXOUT Calculates distance to nearest via hole (X and V are user defined)	2-10

PLEASE USE HYBRID TABLE

SPACING CONSTRAINT SET ASSIGNMENT, CLASS-CLASS

CLASS TO CLASS SPACING		
CLASS NAME	CLASS NAME	CONSTRAINT SET
CIO_D2R	GROUND	DEFAULT_WITH_4X_TO_SHAPE
CIO_R2D	GROUND	DEFAULT_WITH_4X_TO_SHAPE
LPDP	GROUND	DEFAULT_WITH_4X_TO_SHAPE
LPDP_FTCAM	GROUND	DEFAULT_WITH_4X_TO_SHAPE
PCIE_CLK	GROUND	DEFAULT_WITH_4X_TO_SHAPE
PCIE_NAND_D2R	GROUND	DEFAULT_WITH_4X_TO_SHAPE
PCIE_NAND_R2D	GROUND	DEFAULT_WITH_4X_TO_SHAPE
PCIE_WLBT_D2R	GROUND	DEFAULT_WITH_4X_TO_SHAPE
PCIE_WLBT_R2D	GROUND	DEFAULT_WITH_4X_TO_SHAPE
CIO_D2R	POWER	DEFAULT_WITH_4X_TO_SHAPE
CIO_R2D	POWER	DEFAULT_WITH_4X_TO_SHAPE
LPDP	POWER	DEFAULT_WITH_4X_TO_SHAPE
LPDP_FTCAM	POWER	DEFAULT_WITH_4X_TO_SHAPE
PCIE_CLK	POWER	DEFAULT_WITH_4X_TO_SHAPE
PCIE_NAND_D2R	POWER	DEFAULT_WITH_4X_TO_SHAPE
PCIE_NAND_R2D	POWER	DEFAULT_WITH_4X_TO_SHAPE
PCIE_WLBT_D2R	POWER	DEFAULT_WITH_4X_TO_SHAPE
PCIE_WLBT_R2D	POWER	DEFAULT_WITH_4X_TO_SHAPE
CIO_D2R	CIO_D2R	A_DIELECTRIC_4X
CIO_D2R	PCIE_NAND_D2R	A_DIELECTRIC_4X
CIO_D2R	PCIE_WLBT_D2R	A_DIELECTRIC_4X
CIO_D2R	LPDP_FTCAM	A_DIELECTRIC_4X
CIO_D2R	CIO_R2D	A_DIELECTRIC_7X
PCIE_NAND_D2R	PCIE_NAND_D2R	A_DIELECTRIC_4X
PCIE_NAND_D2R	PCIE_WLBT_D2R	A_DIELECTRIC_4X
PCIE_NAND_D2R	LPDP_FTCAM	A_DIELECTRIC_4X
PCIE_NAND_D2R	PCIE_NAND_R2D	A_DIELECTRIC_7X
PCIE_WLBT_D2R	PCIE_WLBT_R2D	A_DIELECTRIC_4X
PCIE_WLBT_D2R	LPDP_FTCAM	A_DIELECTRIC_4X
CIO_R2D	CIO_R2D	A_DIELECTRIC_4X
CIO_R2D	PCIE_NAND_R2D	A_DIELECTRIC_4X
CIO_R2D	PCIE_WLBT_R2D	A_DIELECTRIC_4X
CIO_R2D	PCIE_CLK	A_DIELECTRIC_4X
CIO_R2D	LPDP	A_DIELECTRIC_4X
PCIE_NAND_R2D	PCIE_NAND_R2D	A_DIELECTRIC_4X
PCIE_NAND_R2D	PCIE_WLBT_R2D	A_DIELECTRIC_4X
PCIE_NAND_R2D	PCIE_CLK	A_DIELECTRIC_4X
PCIE_NAND_R2D	LPDP	A_DIELECTRIC_4X
PCIE_WLBT_R2D	PCIE_CLK	A_DIELECTRIC_4X
PCIE_WLBT_R2D	LPDP	A_DIELECTRIC_4X
PCIE_CLK	PCIE_CLK	A_DIELECTRIC_4X
PCIE_CLK	LPDP	A_DIELECTRIC_4X
LPDP	LPDP	A_DIELECTRIC_3X
LPDP_FTCAM	LPDP_FTCAM	A_DIELECTRIC_3X

17.4 SPACING CSETS, CLASS-CLASS

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SOC

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
939-11077	1	PCBA, CORBETT, X2203	U0600	CRITICAL	CPU: INTERPOSER
998-23363	1	IC, DEV, STA, BGA	U0600	CRITICAL	CPU: DEV

B0 BEST

998-26981	1	SOC_STA B0+RG,1Y,10FSTP,LP,BX,H,M2565			U0600	CRITICAL	CPU: SOC_8GB_BEST
998-26978	998-26981	ALT_CMN	ALL	Micron ATK/SCK/ASE			
998-26982	1	SOC_STA B0+16G,1Y,10FSTP,LP,BX,H,M2565			U0600	CRITICAL	CPU: SOC_16GB_BEST
998-26979	998-26982	ALT_CMN	ALL	Micron ATK/SCK/ASE			
998-26984	1	SOC_STA B0+24G,1Z,10FSTP,LP,BX,H,M2565			U0600	CRITICAL	CPU: SOC_24GB_BEST
998-26980	998-26984	ALT_CMN	ALL	Micron ATK/SCK/ASE			

B0 GOOD







998-26988		1	SOC_STA B0+8G,1Y,9FSTP,AP,BX,H,M2565			U0600		CRITICAL		CPU: SOC_8GB_GOOD	
998-26985	998-26988	ALT_CMN	ALL	Micron ATK/SCK/ASE							
998-26981	998-26988	ALT_CMN	ALL	Hynix ATK/SCK/ASE - BEST							
998-26978	998-26988	ALT_CMN	ALL	Micron ATK/SCK/ASE - BEST							
998-26989		1	SOC_STA B0+16G,1Y,9FSTP,AP,BX,H,M2565			U0600		CRITICAL		CPU:SOC_16GB_GOOD	
998-26986	998-26989	ALT_CMN	ALL	Micron ATK/SCK/ASE							
998-26982	998-26989	ALT_CMN	ALL	Hynix ATK/SCK/ASE - BEST							
998-26979	998-26989	ALT_CMN	ALL	Micron ATK/SCK/ASE - BEST							
998-26990		1	SOC_STA B0+24G,1Z,9FSTP,AP,BX,H,M2565			U0600		CRITICAL		CPU:SOC_24GB_GOOD	
998-26987	998-26990	ALT_CMN	ALL	Micron ATK/SCK/ASE							

A1 BEST

998-25075		1	SOC_STA AB+8G,1Y,10C,DEV,RX,H,ATK,M2565			U0600		CRITICAL	CPU: SOC_8GB_BEST_A1
998-25074	998-25075	ALT_CMN	ALL	Hynix SCK					
998-25076	998-25075	ALT_CMN	ALL	Hynix ASE					
998-25077	998-25075	ALT_CMN	ALL	Micron SCK					
998-25078	998-25075	ALT_CMN	ALL	Micron ATK					
998-25079	998-25075	ALT_CMN	ALL	Micron ASE					
998-25081		1	SOC_STA A0+16G,1Y,10C,DEV,RX,H,ATK,M2565			U0600		CRITICAL	CPU: SOC_16GB_BEST_A1
998-25080	998-25081	ALT_CMN	ALL	Hynix SCK					
998-25082	998-25081	ALT_CMN	ALL	Hynix ASE					
998-25083	998-25081	ALT_CMN	ALL	Micron SCK					
998-25084	998-25081	ALT_CMN	ALL	Micron ATK					
998-25085	998-25081	ALT_CMN	ALL	Micron ASE					

A1 GOOD

998-25087		1	SOC_STA A0+8G.1Y.9C.DEV.RX.H.ATK.M2565		U0600		CRITICAL	CPU: SOC_8GB_GOOD_A1
998-25086	998-25087	ALT_CMN	ALL	Hynix SCK				
998-25088	998-25087	ALT_CMN	ALL	Hynix ASE				
998-25089	998-25087	ALT_CMN	ALL	Micron SCK				
998-25090	998-25087	ALT_CMN	ALL	Micron ATK				
998-25091	998-25087	ALT_CMN	ALL	Micron ASE				
998-25075	998-25087	ALT_CMN	ALL	Hynix ATK - BEST				
998-25074	998-25087	ALT_CMN	ALL	Hynix SCK - BEST				
998-25076	998-25087	ALT_CMN	ALL	Hynix ASE - BEST				
998-25077	998-25087	ALT_CMN	ALL	Micron SCK - BEST				
998-25078	998-25087	ALT_CMN	ALL	Micron ATK - BEST				
998-25079	998-25087	ALT_CMN	ALL	Micron ASE - BEST				
998-25093		1	SOC_STA A0+16G.1Y.9C.DEV.RX.H.ATK.M2565		U0600		CRITICAL	CPU: SOC_16GB_GOOD_A1
998-25092	998-25093	ALT_CMN	ALL	Hynix SCK				
998-25094	998-25093	ALT_CMN	ALL	Hynix ASE				
998-25095	998-25093	ALT_CMN	ALL	Micron SCK				
998-25096	998-25093	ALT_CMN	ALL	Micron ATK				
998-25097	998-25093	ALT_CMN	ALL	Micron ASE				
998-25081	998-25093	ALT_CMN	ALL	Hynix ATK - BEST				
998-25080	998-25093	ALT_CMN	ALL	Hynix SCK - BEST				
998-25082	998-25093	ALT_CMN	ALL	Hynix ASE - BEST				
998-25083	998-25093	ALT_CMN	ALL	Micron SCK - BEST				
998-25084	998-25093	ALT_CMN	ALL	Micron ATK - BEST				
998-25085	998-25093	ALT_CMN	ALL	Micron ASE - BEST				

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A Module Parts

RT13 Retimer

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
998-21959	2	IC,LIFORXA,A0,USB-C RETIMER,FCCSP154	UF000,UF100	CRITICAL	ATCRTMR:A0
998-25504	2	IC,LIFORXA,B0,USB-C RETIMER,DEV,CSF154	UF000,UF100	CRITICAL	ATCRTMR:B0

Ace2

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
353802158	3	IC,C203217,ACE2,B2,USB PWR SW W/RT,B0A123	UF400,UF500,U5500	CRITICAL	USBCPC:LAPTOP_B2_PPO
353802742	3	IC,C203217,ACE2,B2,USB PWR SW W/RT,B0A123	UF400,UF500,U5500	CRITICAL	USBCPC:LAPTOP_B2
353802993	3	IC,ACE2,B3,USB PWR SW W/RT,B0A123	UF400,UF500,U5500	CRITICAL	USBCPC:LAPTOP_B3

eUSB Level Shifter

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
338800628	2	IC,FA8890T,C02E2468,B0 L881,OTF-6,C8P25	UF600,UF650	CRITICAL	EUSB_LS:B0

Re-timer Sequencer

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
343800483	2	IC,SLG48AP44593,PMR RAIL SEQUENCER,QPM8	UF790	CRITICAL	

SECURE ELEMENT

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
338800629	1	IC,SN210V,B1,CERES,DEV,VER=LN,MLCSP81	U5000	CRITICAL	SE:DEV_SW_LN
338800630	1	IC,SN210V,B1,CERES,PROD,VER=MD,MLCSP81	U5000	CRITICAL	SE:PROD_SW_MD

B Programmable Parts

USBC ACE2 ROM

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)		CRITICAL	BOM OPTION
335800133	1	IC,SPI SERIAL FLASH,8MBITS,3.0V,US088	UF260		CRITICAL	UPC01_ROM:BLANK
		PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
		335800537	335800133	UPC01_ROM:BLANK	UF260	rdar://80303180
		335800570	335800133	UPC01_ROM:BLANK	UF260	rdar://80303180
		335800571	335800133	UPC01_ROM:BLANK	UF260	rdar://80303180
341801912	1	ROM,ACE-P01 (V2.112.0.5) PROTO-0,K2203	UF260		CRITICAL	UPC01_ROM:P0
341801998	1	ROM,ACE-P01 (V2.116.0.5) PROTO-2,K2203	UF260		CRITICAL	UPC01_ROM:P2
341802052	1	Description: ROM,ACE-P01 (V2.131.3.6) EVT,K2203	UF260		CRITICAL	UPC01_ROM:EVT

MagSafe ACE2 ROM

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)		CRITICAL	BOM OPTION
335800133	1	IC,SPI SERIAL FLASH,8MBITS,3.0V,US088	U5560		CRITICAL	UPC5_ROM:BLANK
		PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
		335800537	335800133	UPC5_ROM:BLANK	U5560	rdar://80303078
		335800570	335800133	UPC5_ROM:BLANK	U5560	rdar://80303078
		335800571	335800133	UPC5_ROM:BLANK	U5560	rdar://80303078
341801913	1	ROM,ACE-P5 (V2.112.0.3) PROTO-0,K2203	U5560		CRITICAL	UPC5_ROM:P0
341801999	1	ROM,ACE-P5 (V2.116.0.3) PROTO-2,K2203	U5560		CRITICAL	UPC5_ROM:P2
341802053	1	ROM,ACE-P5 (V2.131.3.6) EVT,K2203	U5560		CRITICAL	UPC5_ROM:EVT

SOC ROM

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
998-22994	1	IC,FLASH,64MBIT,1.2V,QE=1,M,4X40M,S0N8	U1900	CRITICAL	SOC_ROM:BLANK_P1
335800575	1	IC,FLASH,64MBIT,1.2V,QE=1,M,4X40M,S0N8	U1900	CRITICAL	SOC_ROM:BLANK


RT13 ROM(s)

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)		CRITICAL	BOM OPTION
998-22993	2	IC_FLASH,64MBIT,1.2V,QE=1,M,4X40M,S0N8	UF090,UF190		CRITICAL	RT13_ROM:BLANK_P1
335800574	2	IC_FLASH,64MBIT,1.2V,QE=1,M,4X40M,S0N8	UF090,UF190		CRITICAL	RT13_ROM:BLANK
	PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:	
	335800575	335800574	RT13_ROM:BLANK	UF090,UF190	rdar://76779010	

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BOM: Prog and Module Parts

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	998-23585	1	IC,PMU,VALE,CSP196		U7700	CRITICAL	SPMU_IC:DEV									
	998-24583	1	IC,PMU,VALE,A0,OTP-JPC,CSP196		U7700	CRITICAL	SPMU_IC:A0_JPC									
	998-25434	1	IC,PMU,VALE,A0,OTP-JPD,WLCSP196		U7700	CRITICAL	SPMU_IC:A0_JPD									
	998-26179	1	IC,PMU,VALE,A0,OTP-JPE,WLCSP196		U7700	CRITICAL	SPMU_IC:A0_JPE									
	998-26198	1	IC,PMU,VALE,A0,OTP-JPF,WLCSP196		U7700	CRITICAL	SPMU_IC:A0_JPF									
	998-26683	1	IC,PMU,VALE,A0,OTP-JPG,WLCSP196		U7700	CRITICAL	SPMU_IC:A0_JPG									
	998-26878	1	IC,PMU,VALE,A0,OTP-JPH,WLCSP196		U7700	CRITICAL	SPMU_IC:A0_JPH									
	998-27502	1	IC,PMU,VALE,A0,OTP-JPI,WLCSP196		U7700	CRITICAL	SPMU_IC:A0_JPI									
C	MPMU															C
	PART NUMBER	QTY	DESCRIPTION		REFERENCE DES	CRITICAL	BOM OPTION									
	998-23524	1	IC,PMU,STOWE,CSP420		U8100	CRITICAL	MPMU_IC:DEV									
	998-24581	1	IC,PMU,STOWE,A0,OTP-JPC,CSP420		U8100	CRITICAL	MPMU_IC:A0_JPC									
	998-25433	1	IC,PMU,STOWE,A0,OTP-JPD,WLCSP420		U8100	CRITICAL	MPMU_IC:A0_JPD									
	998-26178	1	IC,PMU,STOWE,A0,OTP-JPE,WLCSP420		U8100	CRITICAL	MPMU_IC:A0_JPE									
	998-26197	1	IC,PMU,STOWE,A0,OTP-JPF,WLCSP420		U8100	CRITICAL	MPMU_IC:A0_JPF									
	998-26682	1	IC,PMU,STOWE,A0,OTP-JPG,WLCSP420		U8100	CRITICAL	MPMU_IC:A0_JPG									
	998-26877	1	IC,PMU,STOWE,A0,OTP-JPH,WLCSP420		U8100	CRITICAL	MPMU_IC:A0_JPH									
	998-27501	1	IC,PMU,STOWE,A0,OTP-JPI,WLCSP420		U8100	CRITICAL	MPMU_IC:A0_JPI									
B																B
A																A

